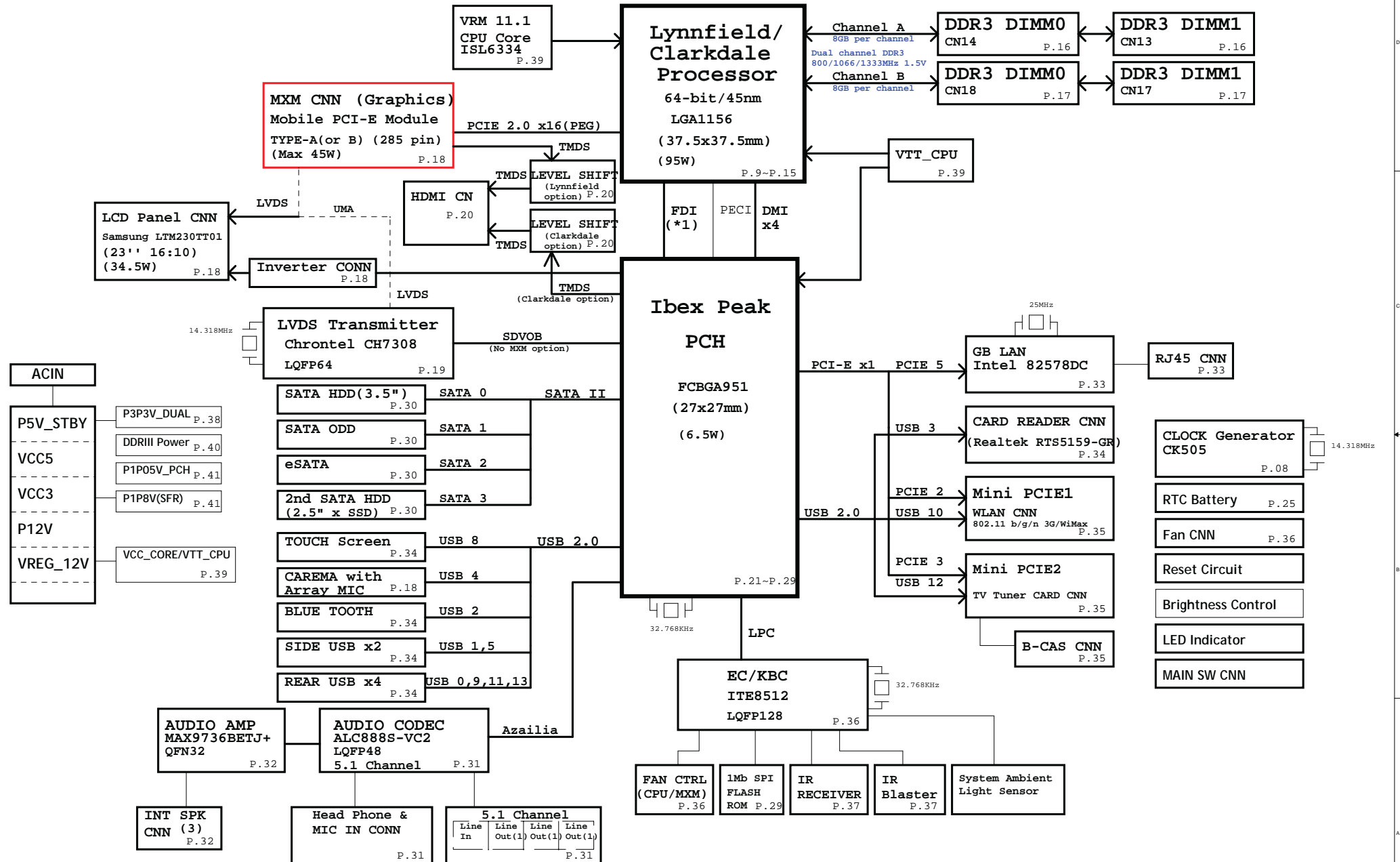


EL5 Block Diagram :



FDI - Used only for the Clarkdale processor.

Net name Description :

Voltage Rails

P5V_STBY	5.0V always on power rail by LATCH or ACIN
P3P3V_STBY	3.3V always on power rail by LATCH or ACIN
P1P5V	1.5V switched power rail by SUSB#/PM_SLP_S3#
P2P5V	2.5V switched power rail by SUSB#/PM_SLP_S3#
VCC3	3.3V switched power rail by SUSB#/PM_SLP_S3#
VCC5	5.0V switched power rail by SUSB#/PM_SLP_S3#
P12V	12V switched power rail by SUSB#/PM_SLP_S3#
VREG_12V	12V switched power rail for CPU Vcore
VCCP	Core Voltage for CPU
P1V1_CPU_VTT	1.1V power rail for AGTL+ termination & PCH DMI I/F by SUSB#/PM_SLP_S3#
P1P05V_PCH	1.05V power rail for PCH Core;PCH I/O;DMI;PCIE;SATA by SUSB#/PM_SLP_S3#
P1P8_SFR	1.8V power rail for CPU PLL & PCH NAND I/F by SUSC#/PM_SLP_S4#
P1P5V_SUS	1.5V power rail for DDRIII by SUSC#/PM_SLP_S4#
0.75VDDT_DDR3	0.75V DDRIII Termination Voltage by SUSB#/PM_SLP_S3#

Part Naming Conventions

- C = Capacitor
- CN = Connector
- D = Diode
- F = Fuse
- L = Inductor
- Q = Transistor
- R = Resistor
- RP = Resistor Pack
- U = Arbitrary Logic Device
- Y = Crystal and Osc

Net Name Suffix

or _N = Active Low signal

Board Stack up Description

02

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Power Plane
Layer 3		Normal Signal / Ground 1 Plane
Layer 4		Stripline Layer(High Speed)
Layer 5		Ground Plane
Layer 6		Solder Side, Microstrip signal Layer

Layers : 6 Depth 1.2mm Impence 55 ohms +/- 10%

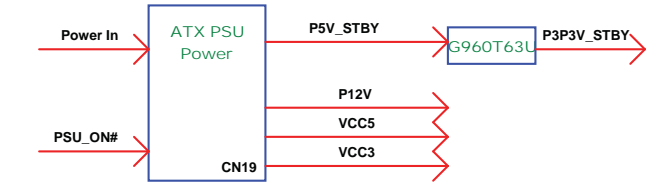
	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR3 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR3 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR3 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
Lan	50 ohm +/- 15%		

For no M3 support with Intel LAN:

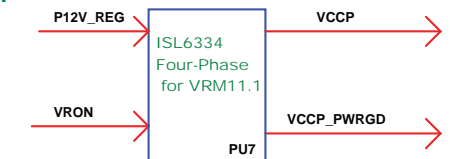
- 1.05 V ME powered by 1.05 V PCH
- 3.3 V SPI (3.3 V EPW) powered by 3.3 V Main
- VCCLAN (LAN MAC well) is powered by 1.05 ME well (which is powered by 1.05 PCH)
- VCCLANPHY power is gated by SLP_LAN#

Power rail control

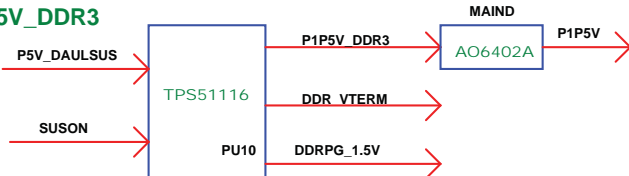
PSU



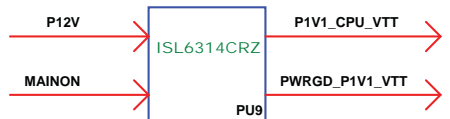
VCCP



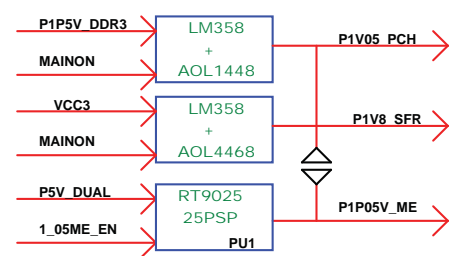
P1P5V_DDR3



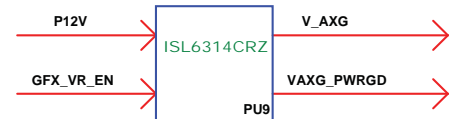
P1V1_CPU_VTT



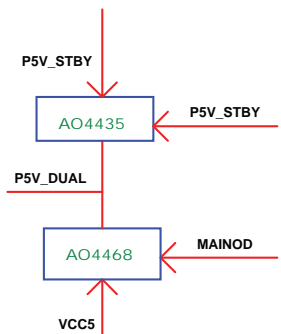
P1V05_PCH/P1V8_SFR/P1P05V_ME



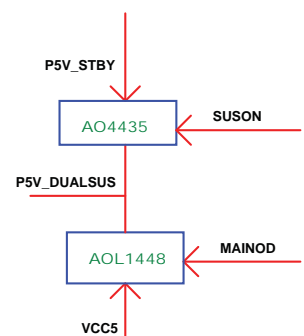
V_AXG



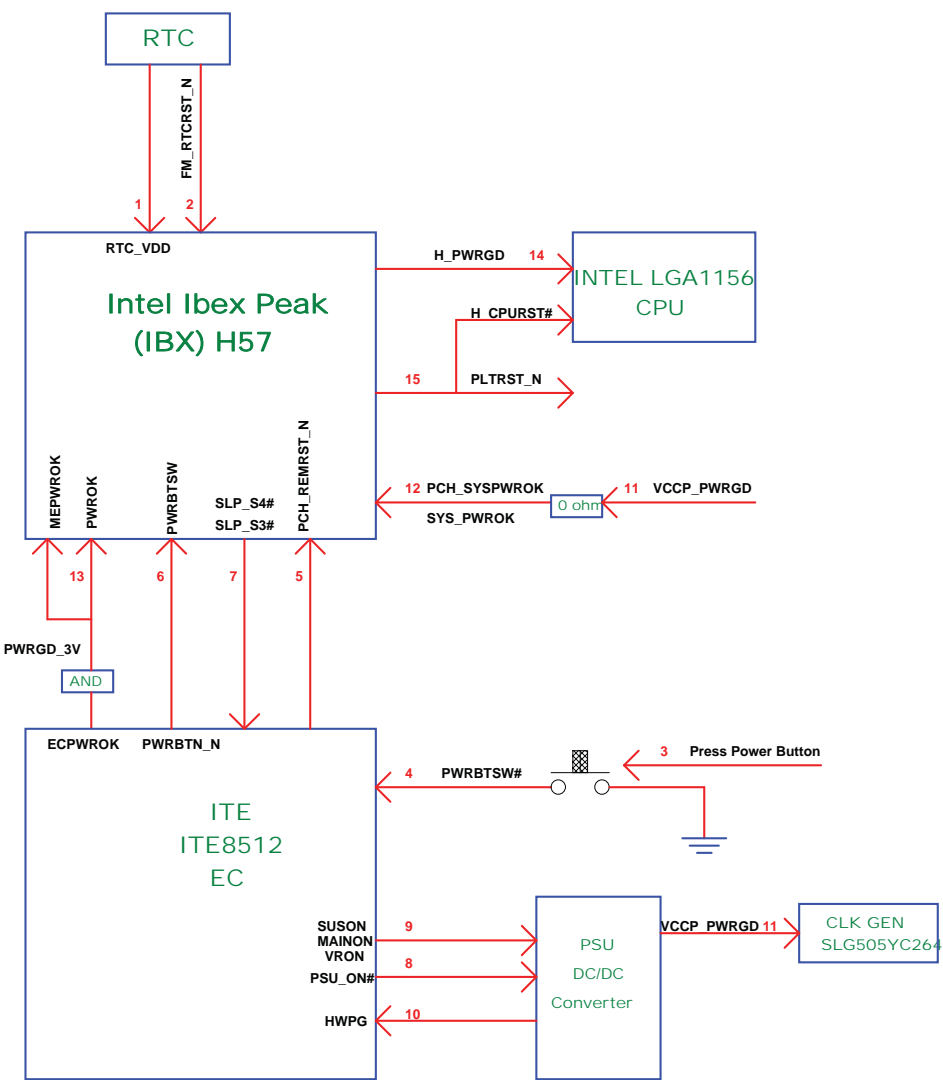
P5V_DUAL



P5V_DUALSUS

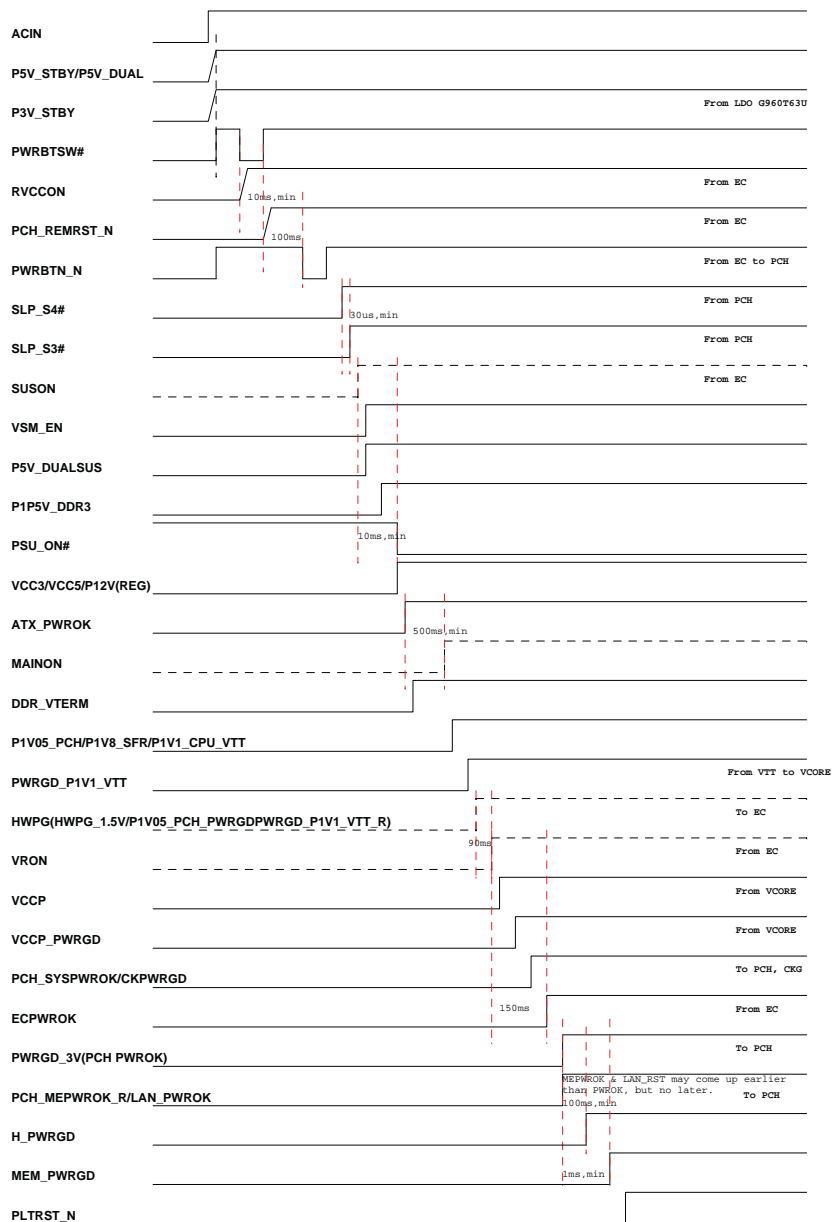


Power on Sequence

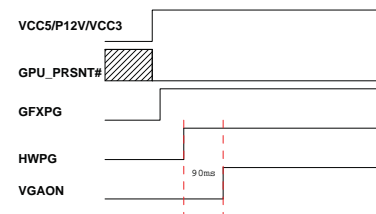


Power on Sequence :

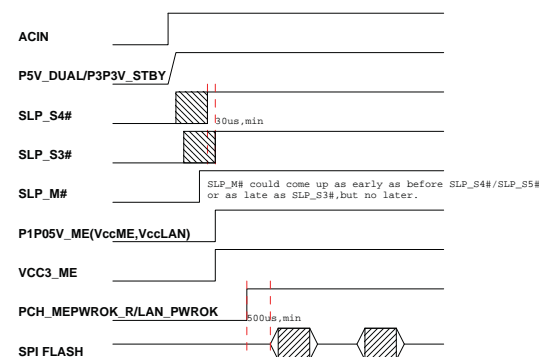
04



MXM POWER ON



SLP_M#, M3 ON



Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Lynnfield : Default for initial power up	0.65V~1.4V 1.1V	90A(TDC) Max:110A
VTT_CPU	Lynnfield : Memory controller & shared cache Ibex Peak : DMI Ibex Peak : CPU_IO	1.045V~1.1V~1.155V 1.1V 1.05V~1.1V~1.16V	30A(TDC) Max: 35A 0.065A 0.001A
P1P8V(SFR)	Lynnfield : Internal processor PLL Ibex Peak : Internal PLL & VRMs Ibex Peak : Dual channel NAND I/F NVRAM : VCCQ NVRAM : VREF	1.71V~1.8V~1.89V 1.71V~1.8V~1.89V 1.71V~1.8V~1.89V	1.1A 0.196A 0.156A
P1P5V_SUS	Lynnfield : CPU I/O Voltage for DDRIII DIMM :	1.425V~1.5V~1.575V	6A
0.75VDDT_DDR3	DDRIII Terminator:	0.75V	?A
P1P05V_PCH	Ibex Peak : VccCore Ibex Peak : Vcc core I/O buffer Ibex Peak : DMI buffer voltage Ibex Peak : Intel Management Engine Ibex Peak : Display PLL A power Ibex Peak : Display PLL B power Ibex Peak : LAN	0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V 0.998V~1.05V~1.1V	1.629A 3.251A 0.065A 2.222A 0.075A 0.075A 0.372A
P1P5V	Mini PCIE : +1.5V(WLAN) Mini PCIE : +1.5V(TV)		
P2P5V	CH7308 : DVDD		
VCC3	Ibex Peak : I/O buffer voltage Ibex Peak : Display DAC Analog power CLK Gen.CK505 : VDD NVRAM : VCC MXM : 3V3 CH7308 : LVDD ALC888S : DVDD Mini PCIE : +3.3V(WLAN) Mini PCIE : +3.3V(TV) Bluetooth : +3.3V Media Card : +3.3V(JMB385) EC(IT8512) : VCC CAREMA	3.14V~3.3V~3.47V 3.14V~3.3V~3.47V	0.357A 0.069A
VCC5	Ibex Peak : Core well Ref. voltage MXM : 5V SATA ODD SATA HDD(2.5" x SSD) ALC888S : AVDD Audio AMP(MAX9736BETJ) : Touch Screen LCD Panel USB: x 5 ports	4.75V~5V~5.25V 5V	0.001A 2.5A
P3P3V_STBY	Ibex Peak : Intel Management Engine Ibex Peak : Suspend well I/O Buffer Ibex Peak : HD Audio controller Suspend Voltage LAN RTL8111DL : VDD IR Receiver EC(IT8512) : VSTBY SPI FLASH ROM	3.14V~3.3V~3.47V 3.14V~3.3V~3.47V 3.14V~3.3V~3.47V	0.086A 0.168A 0.006A
P5V_STBY	Ibex Peak : Suspend well Ref. Voltage	4.75V~5V~5.25V	0.001A
P12V	MXM : 12V INVERTER : Vin FAN_CPU FAN_MXM Audio AMP(MAX9736BETJ) : PVDD		

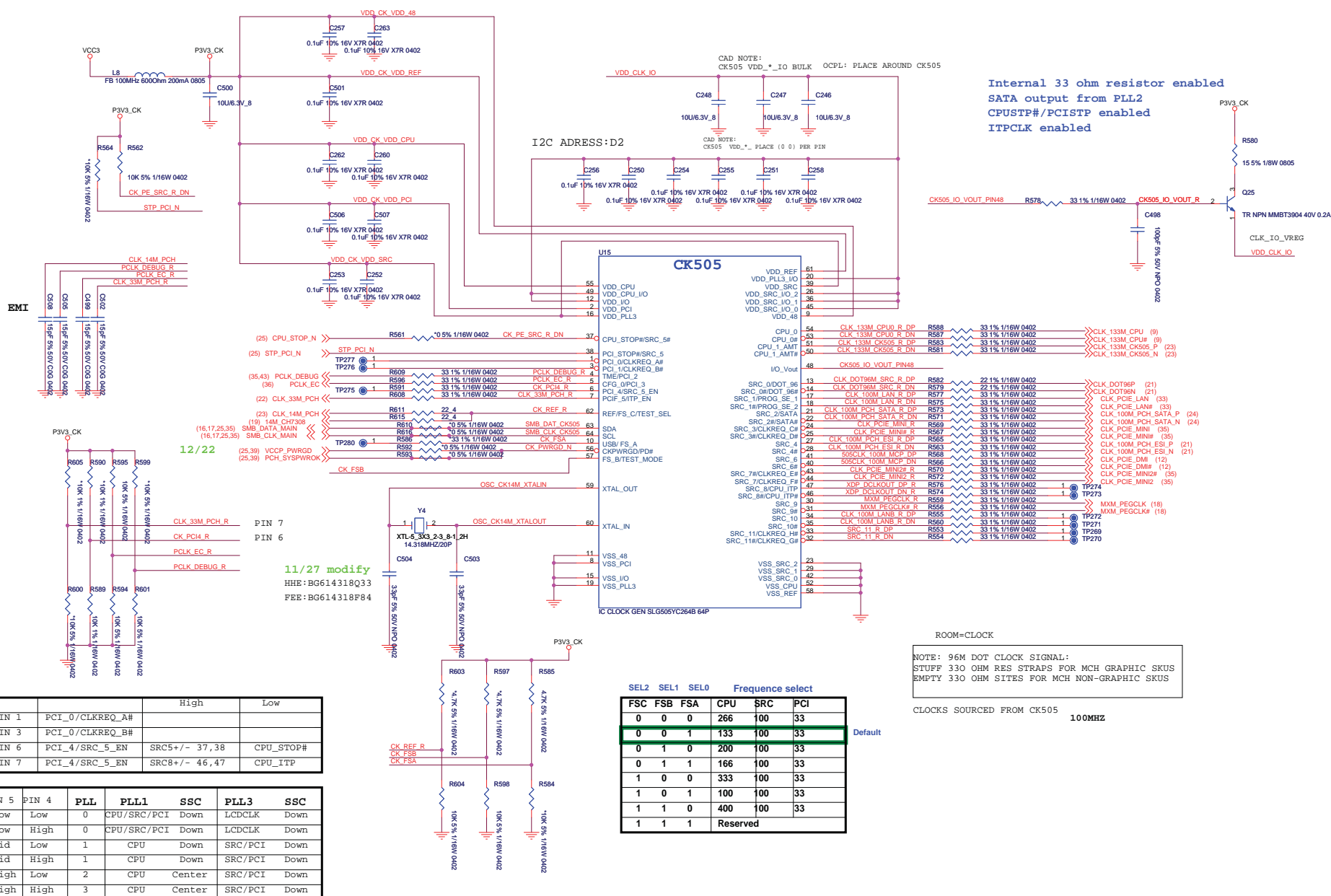
Schmatic Change List:

06

Date	Change Item Description	Note
11/13	1.PAGE25 ADD R766 SLP_S4#	
	2.PAGE29 ADD R767、R768、R769	
11/24	1.PAGE38 ADD PC179、PR157	
11/26	1.PAGE9 ADD C601、C602、C603、R770、R771	
11/30	1.PAGE34 ADD R772、C604	
12/01	1.PAGE18 Del R49、R53、R54、C120、Add U2、R773、R774、R775、R776、C605、C606、C607、C608、U26、Q46。For EDID	
12/03	1.PAGE41 Add PR85、PR158	
	2.PAGE19 Add PU12、PR159、PR160、PR161、PC180、PC181、PC182、PC183、PC184 For P2P5V	
	3.PAGE20 Add U25、L29、R49、R54、R55、R67、R68、R349、R681、R682、R712、R724、R725、R779、R780、R781、R782、R783、R784、R785、R786、R787、R788、R789、R790、R791、R792、R793、C19、C21、C22、C120、C609、C610、C611 for MXM HDMI Repeater	
12/04	1.PAGE18 Add C617	
VER:C		
12/22	1.PAGE18 Del U26、R774、C606、Q46、C608、R776、R773、R775、C605、C607,Add R318、R696、R314、C605。For EDID	
	2.PAGE34 Change CN33 to 5PIN CONN	
01/05	1.PAGE39 Add PR163、R800、R801。	
01/07	1.PAGE34 Del R1、R2、Add L30。For EMI	
	2.PAGE33 ADD R802、D47。For LAN Wake up	
	3.PAGE40 PC160 connector to P1P5V_DDR3。	
01/11	1.PAGE35 Add R803、R804、R805、R806。For PCI_E detect	
	2.PAGE33 Add R807。For LAN LED	
VER:D		

Schmatic Change List:

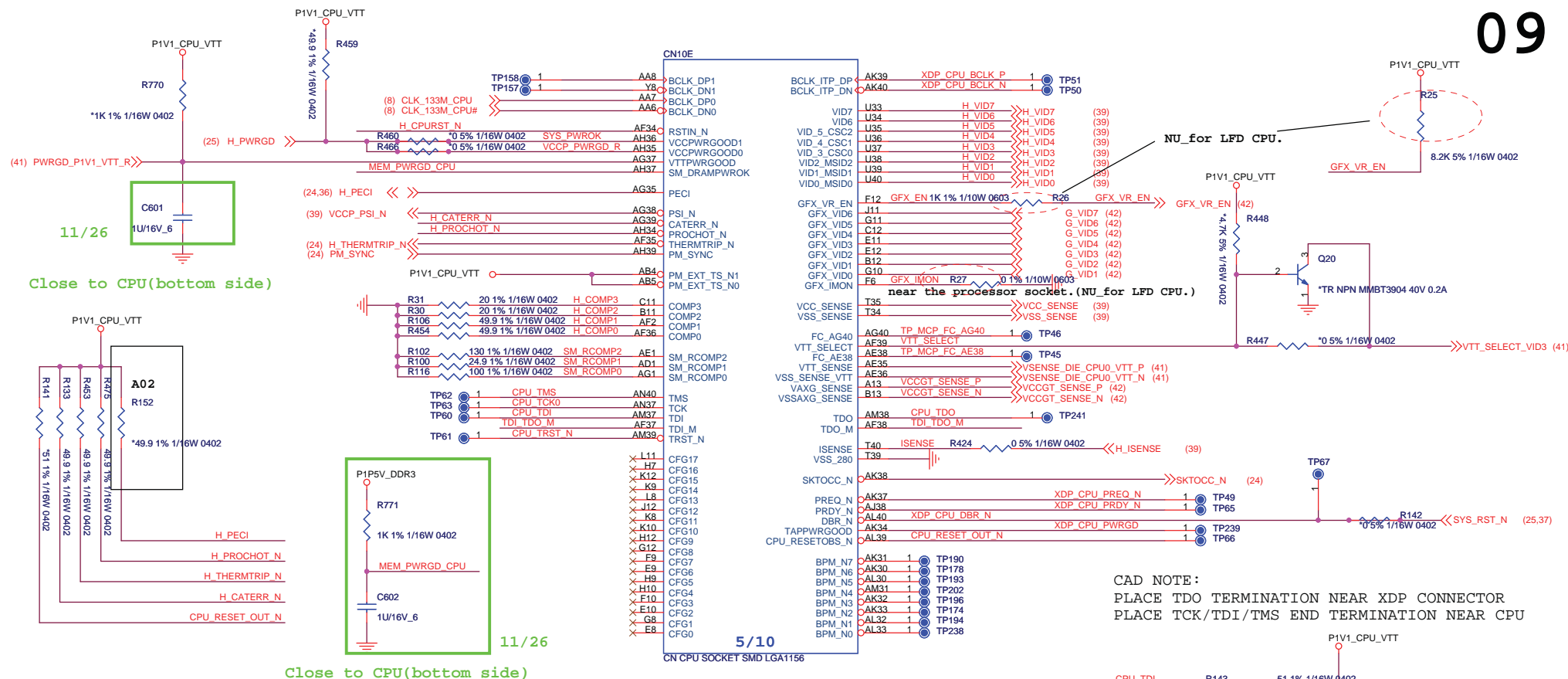
Date	Change Item Description	Note



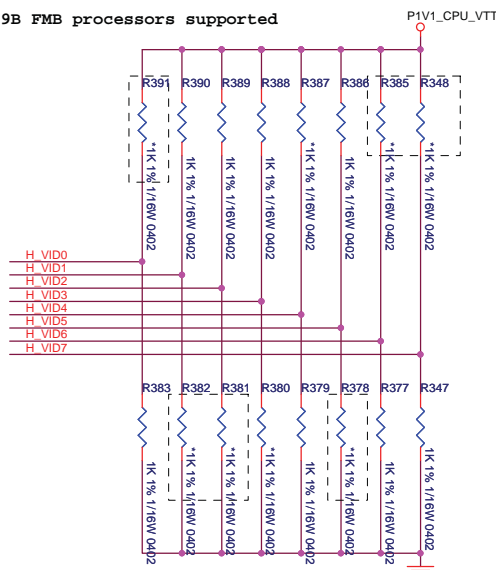
		High	Low
PIN 1	PCI_0/CLKREQ_A#		
PIN 3	PCI_0/CLKREQ_B#		
PIN 6	PCI_4/SRC_5_EN	SRC5+/- 37,38	CPU_STOP#
PIN 7	PCI_4/SRC_5_EN	SRC8+/- 46,47	CPU_ITP

PIN 5	PIN 4	PLL	PLL1	SSC	PLL3	SSC
Low	Low	0	CPU/SRC/PCI	Down	LCDCCLK	Down
Low	High	0	CPU/SRC/PCI	Down	LCDCCLK	Down
Mid	Low	1	CPU	Down	SRC/PCI	Down
Mid	High	1	CPU	Down	SRC/PCI	Down
High	Low	2	CPU	Center	SRC/PCI	Down
High	High	3	CPU	Center	SRC/PCI	Down

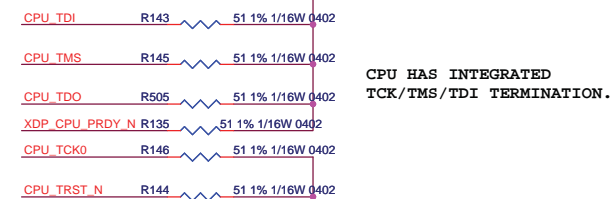
SEL2	SEL1	SEL0	Frequency select		
FSC	FSB	FSA	CPU	SRC	PCI
0	0	0	266	100	33
0	0	1	133	100	33
0	1	0	200	100	33
0	1	1	166	100	33
1	0	0	333	100	33
1	0	1	100	100	33
1	1	0	400	100	33
1	1	1	Reserved		



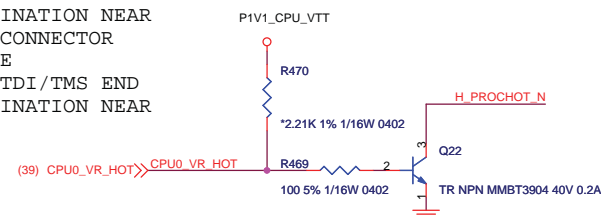
VID[7:0] : 00101110 =>1.325V@VCC,Max
2009B FMB processors supported

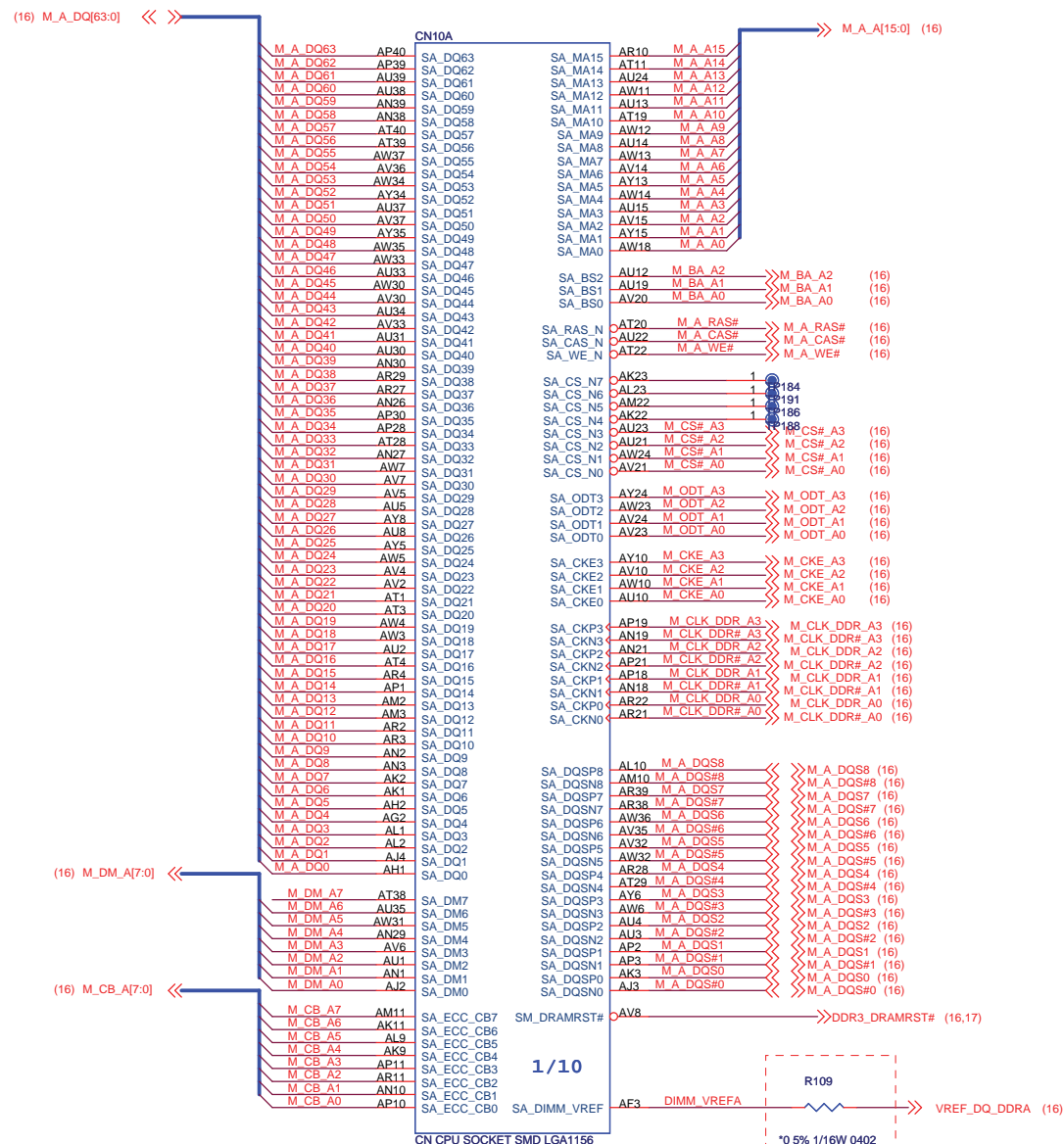


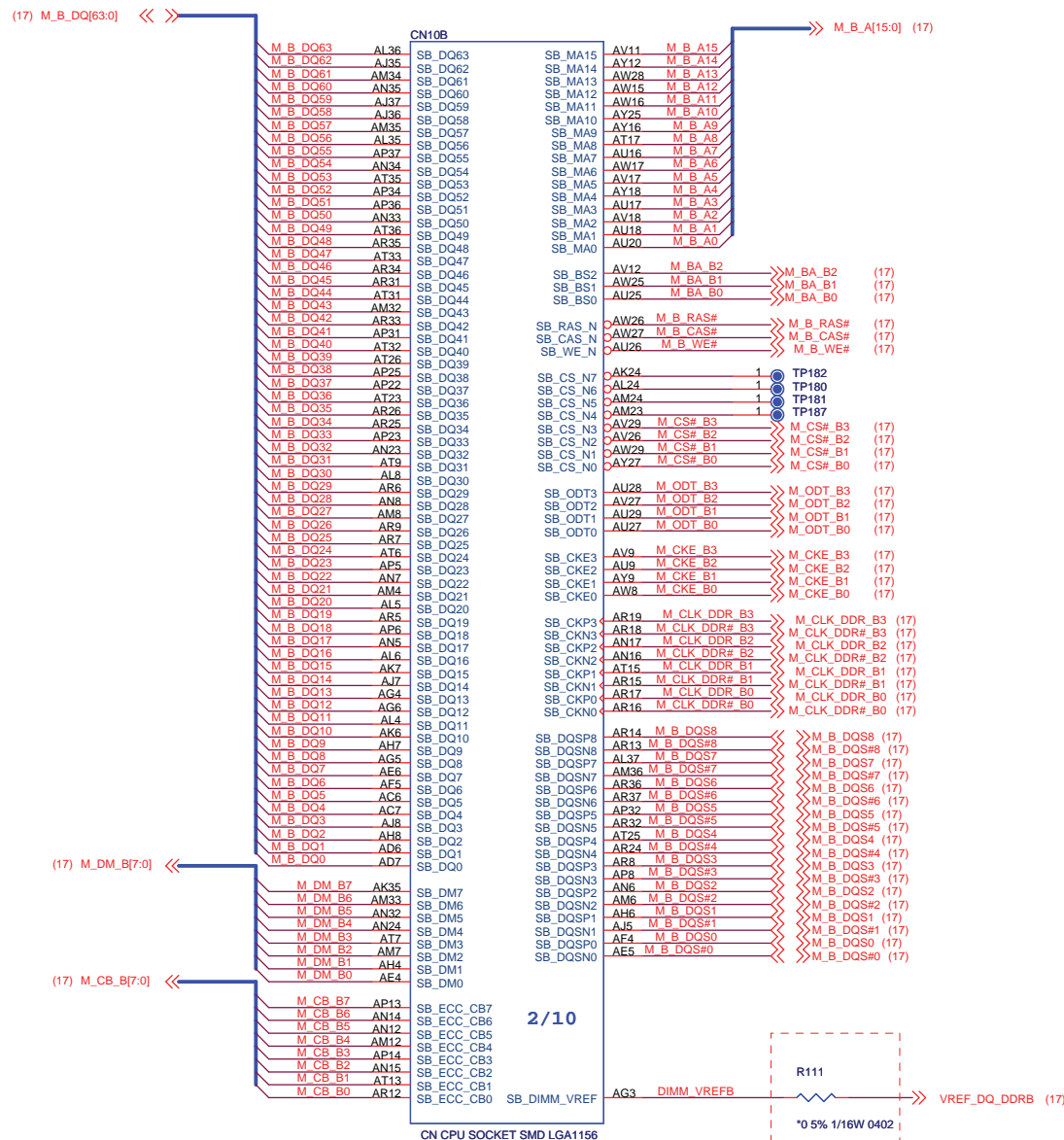
CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU

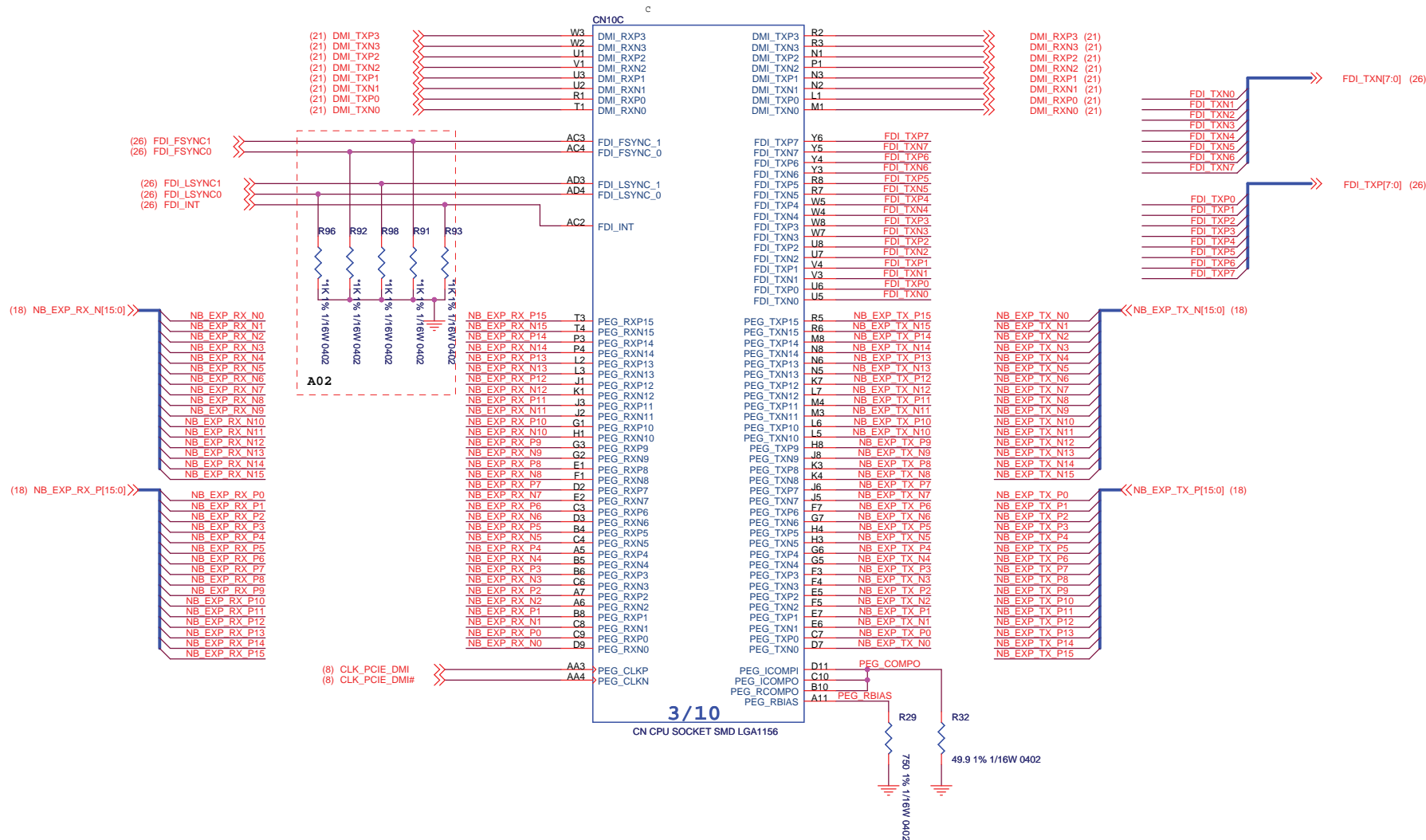


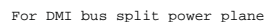
CAD NOTE:
PLACE TDO TERMINATION NEAR XDP CONNECTOR
PLACE TCK/TDI/TMS END TERMINATION NEAR CPU





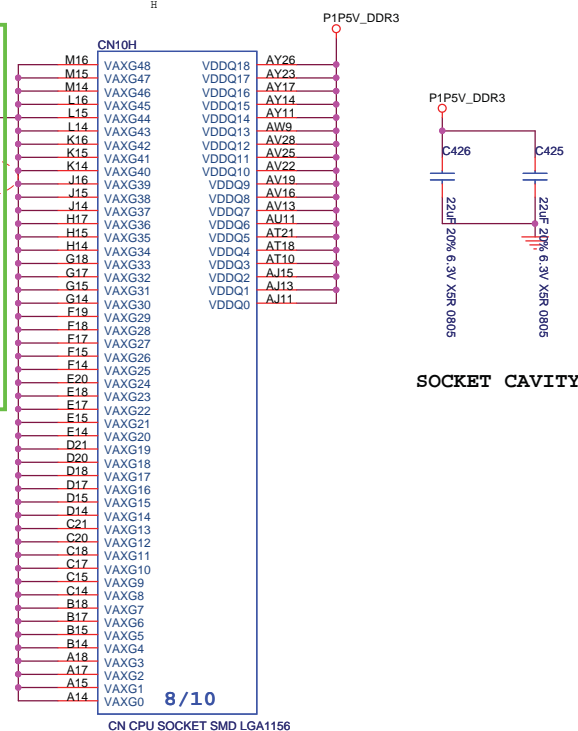
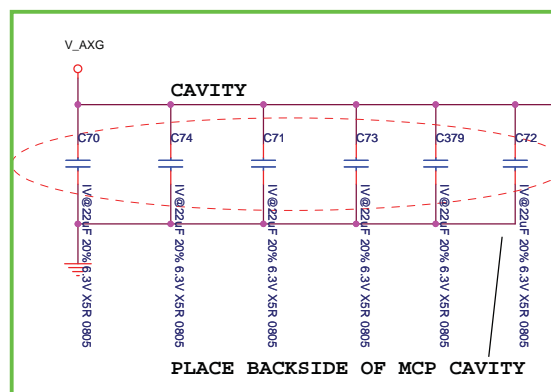
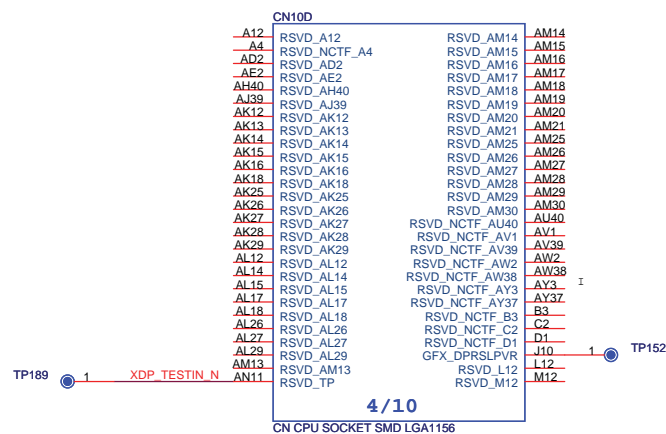






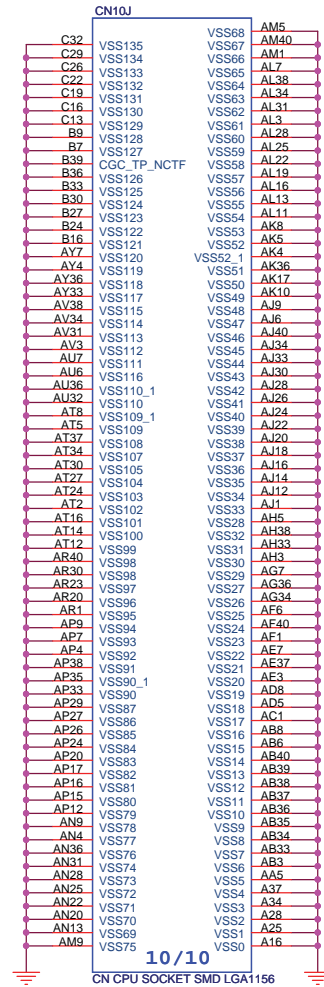
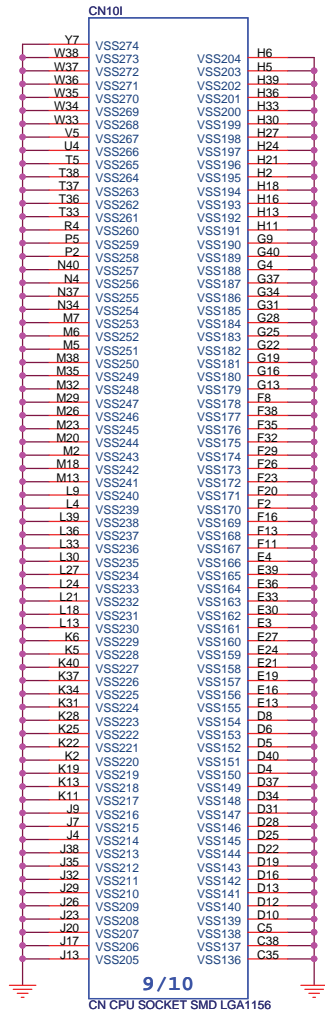
BOM note:
EV@C70、C71、C72、C73、C74、C379 need
to stuff 0ohm RES

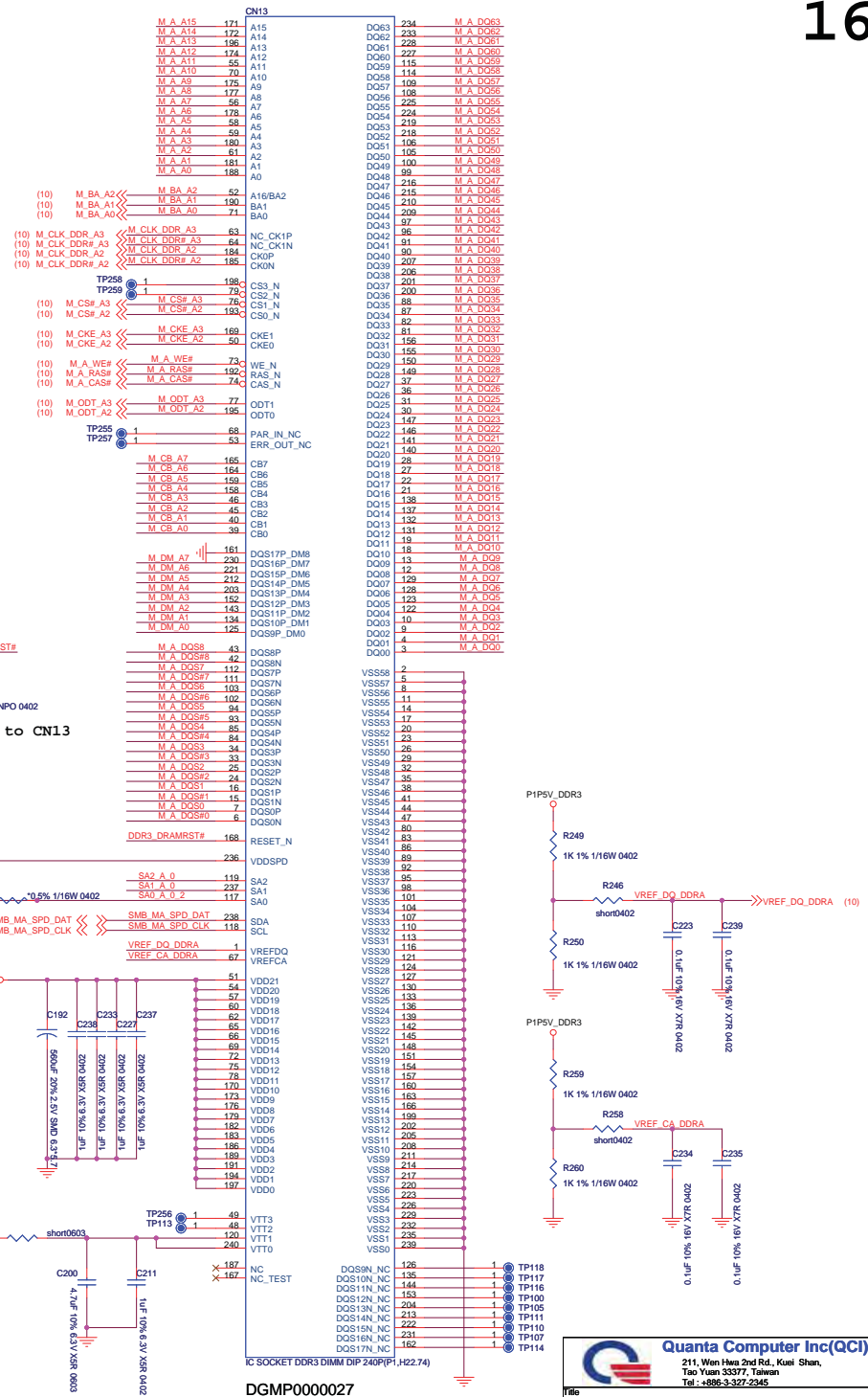
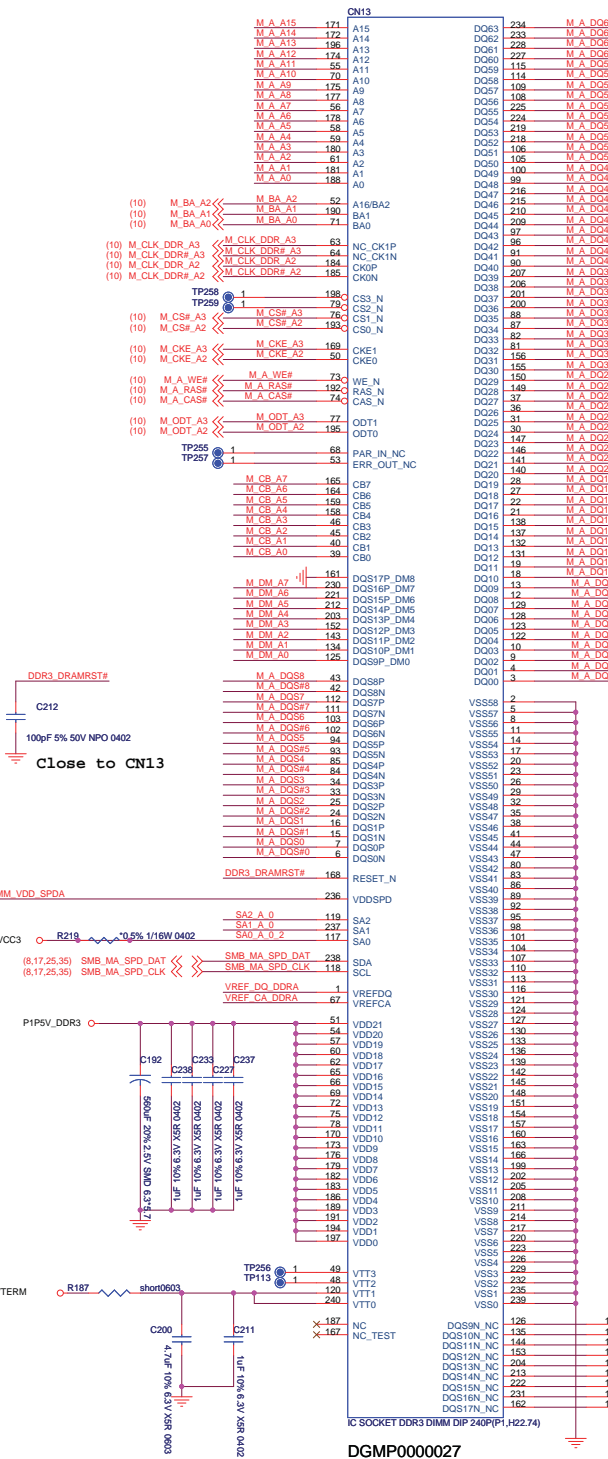
VAXG tie to GND for LFD CPU.



SOCKET CAVITY

Quanta Computer Inc(QCI). 211, Wen Hwa 2nd Rd., Kuei Shan, Tao Yuan 33377, Taiwan Tel.: +886-3-327-2345		Confidential
Title: MCP - V_AXG/ P1P5V_DDR3		
Size: Custom	Document Number: EL5	Rev: A02
Date: Thursday, March 04, 2010		Sheet: 14 of 43

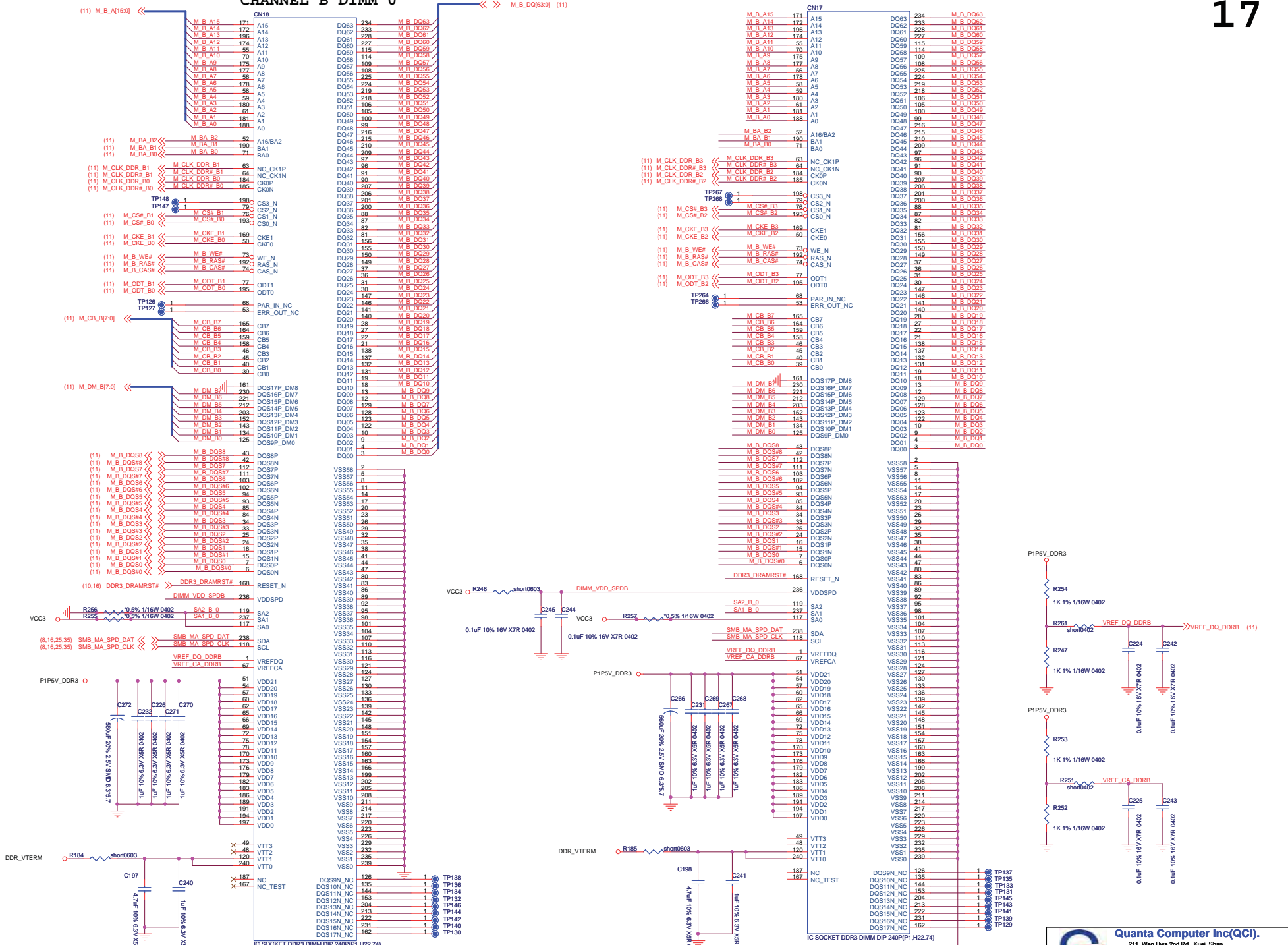




CHANNEL B DIMM 0

CHANNEL B DIMM 1

17

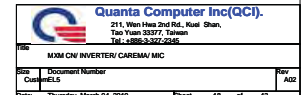


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DGMP0000027

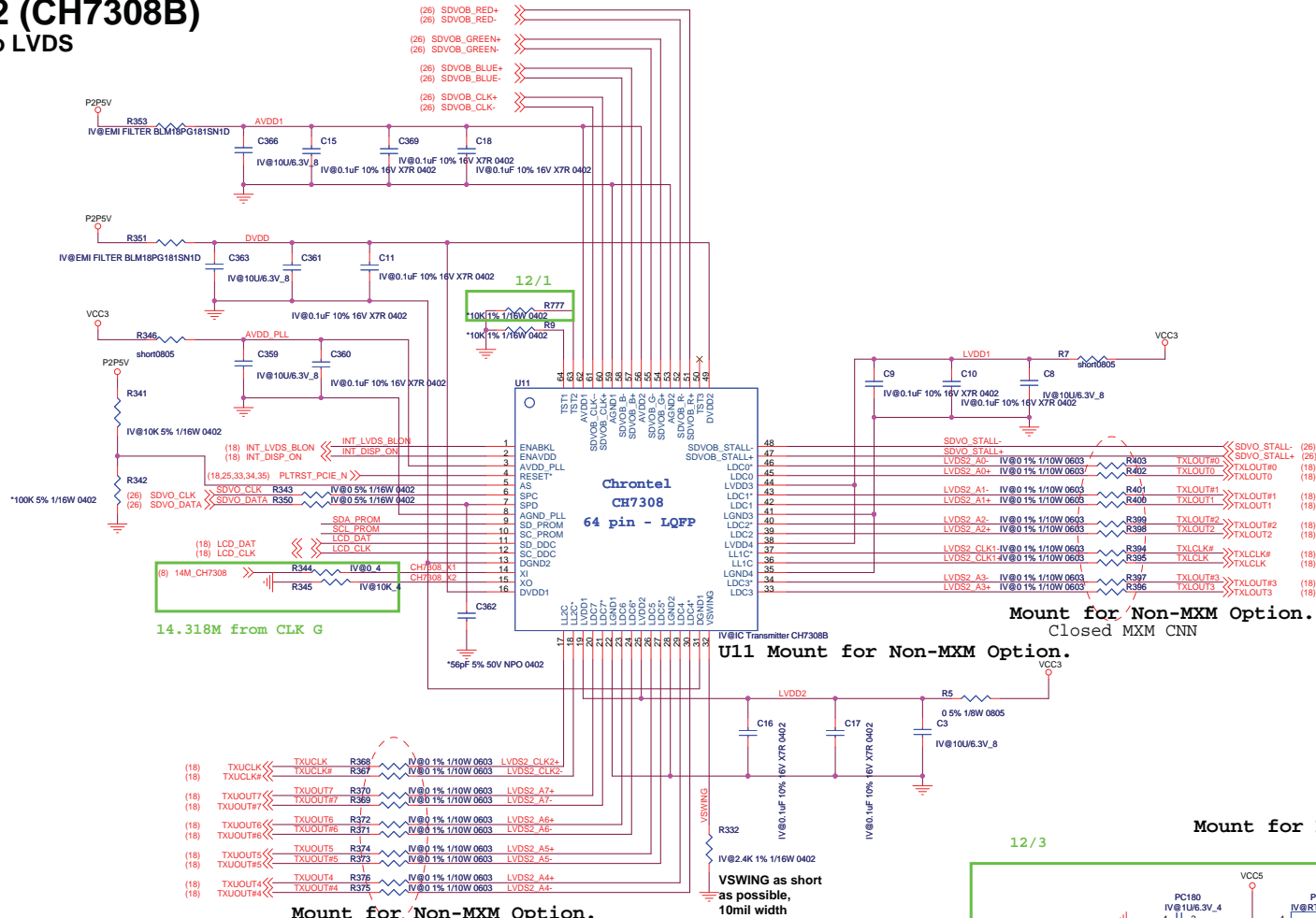
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 211, Wen Hwa 2nd Rd., Kwei Shan,
 Tao Yuan 33377, Taiwan
 Tel: +886-3-372-2345

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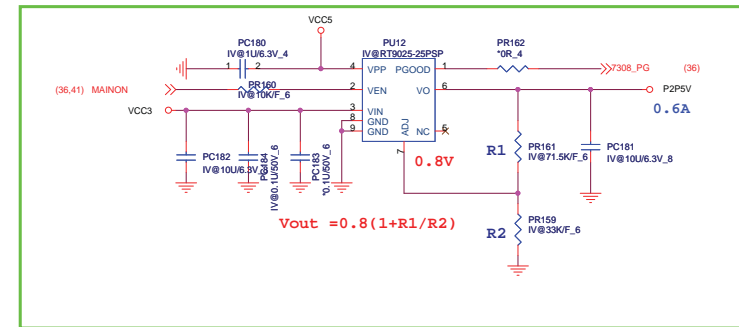
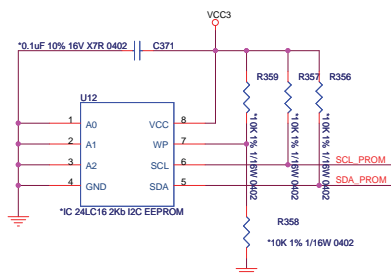


LVDS2 (CH7308B)

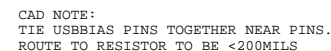
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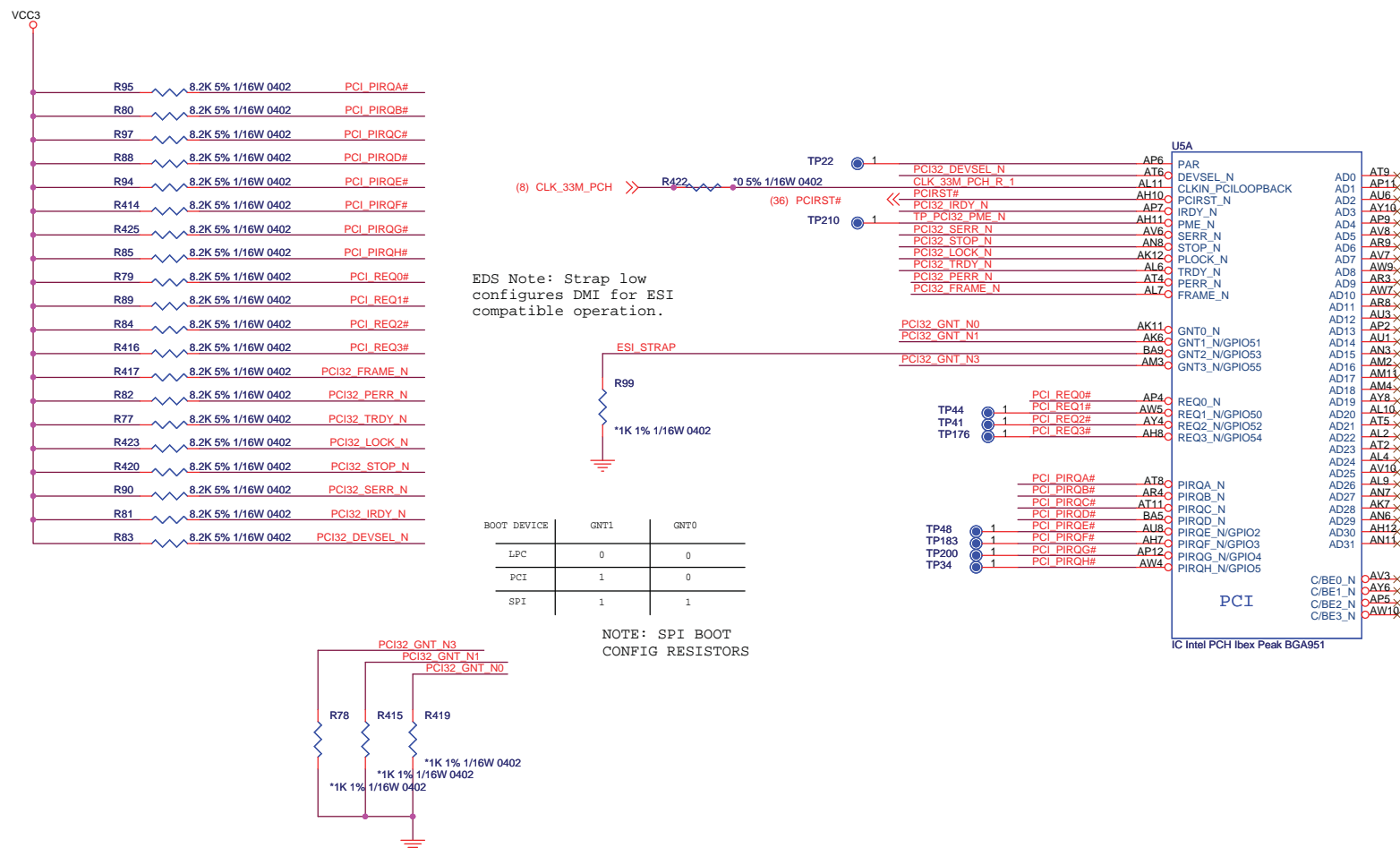


Mount for Non-MXM Option.
Closed MXM CNN



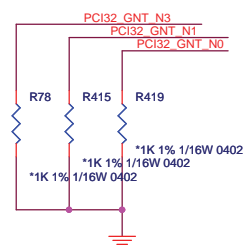




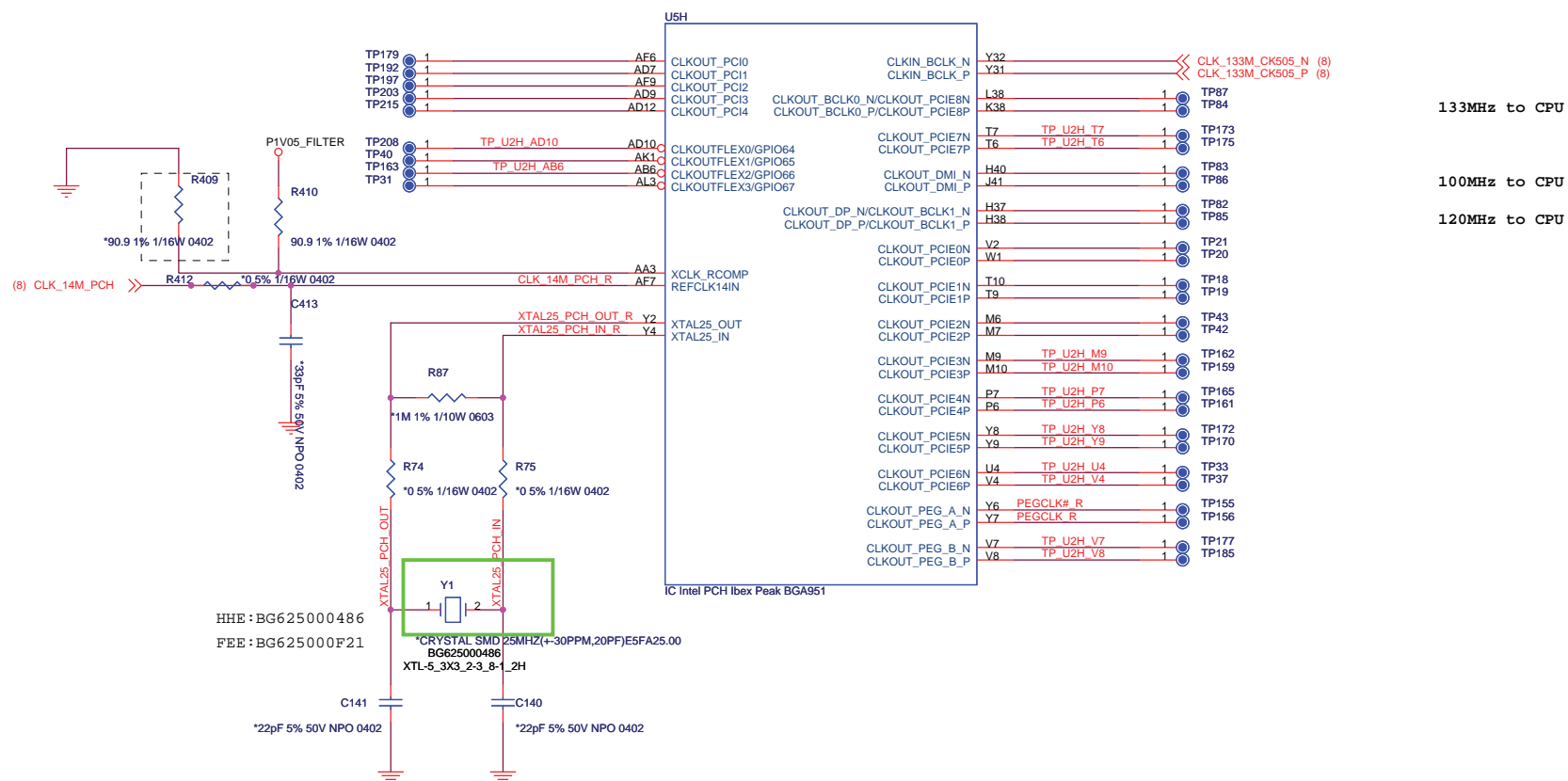


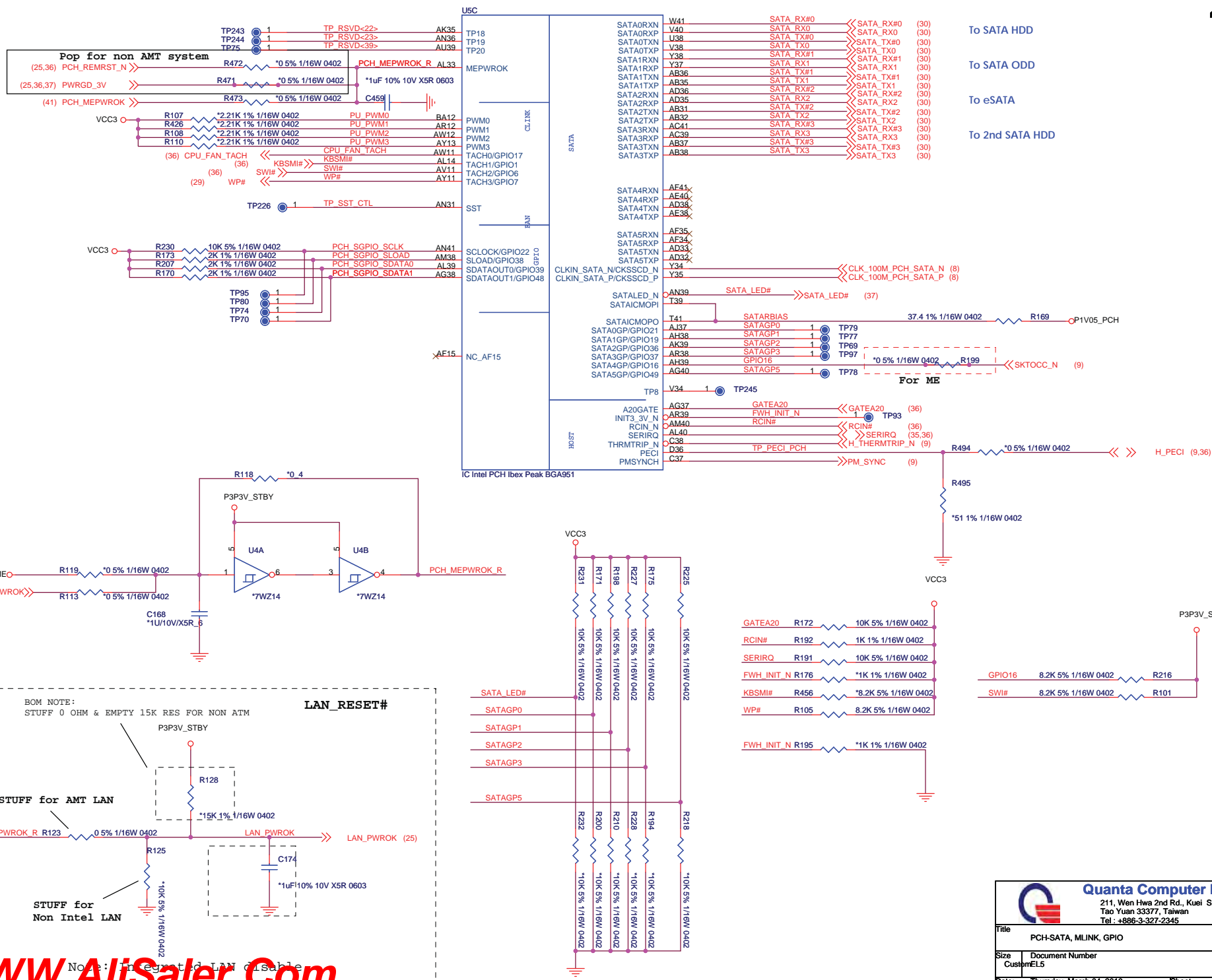
BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	1	0
SPI	1	1

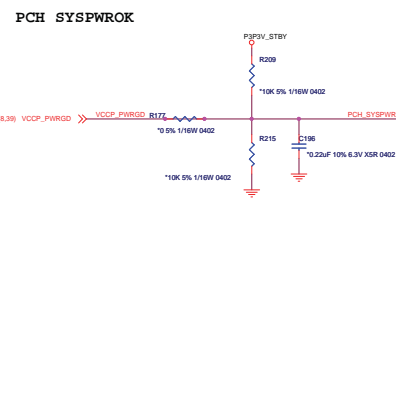
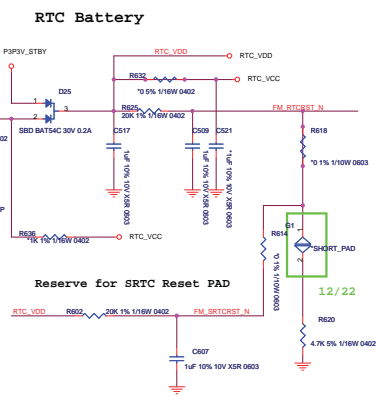
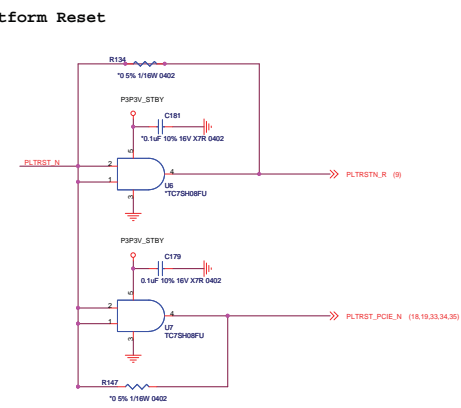
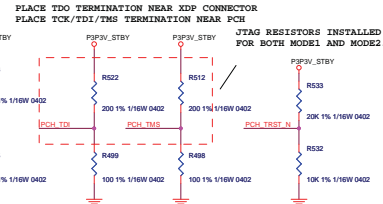
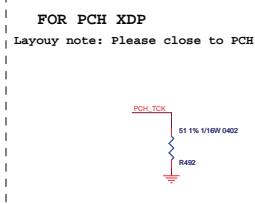
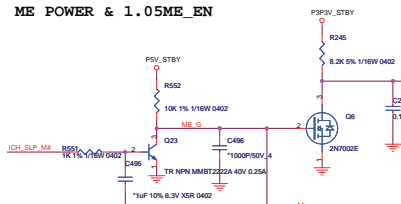
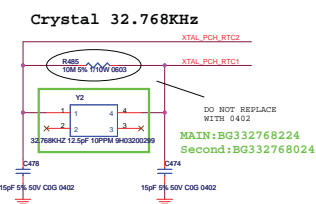
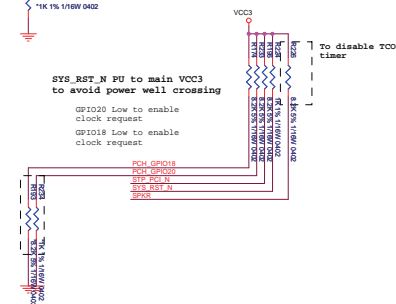
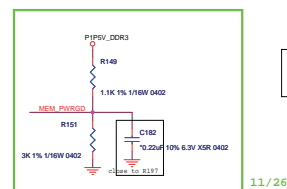
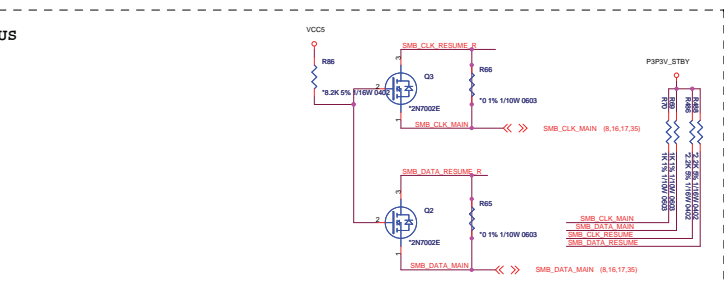
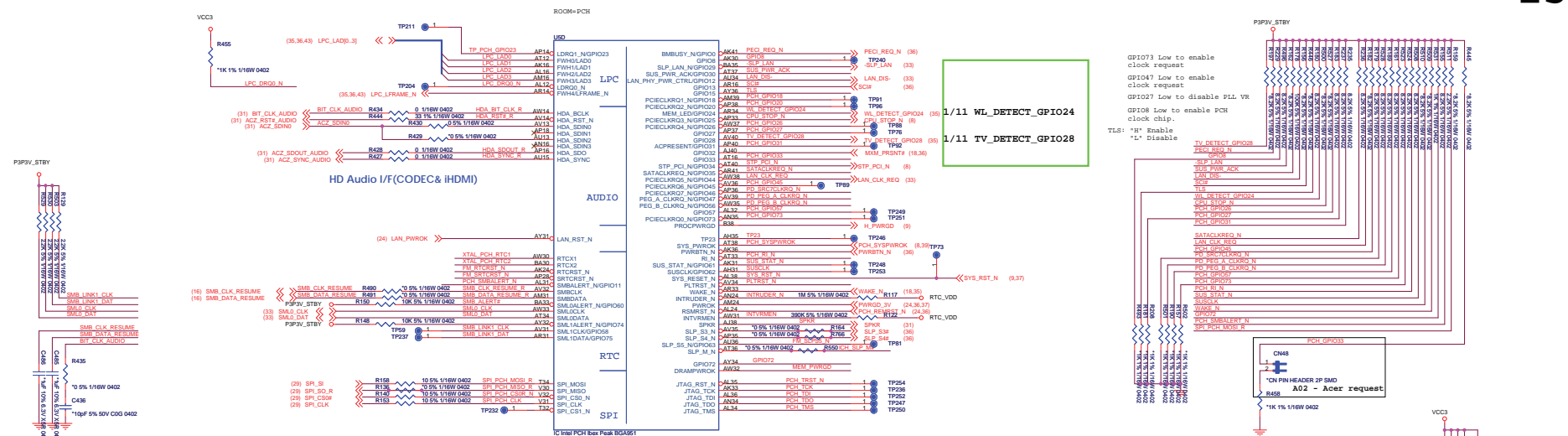
NOTE: SPI BOOT CONFIG RESISTORS

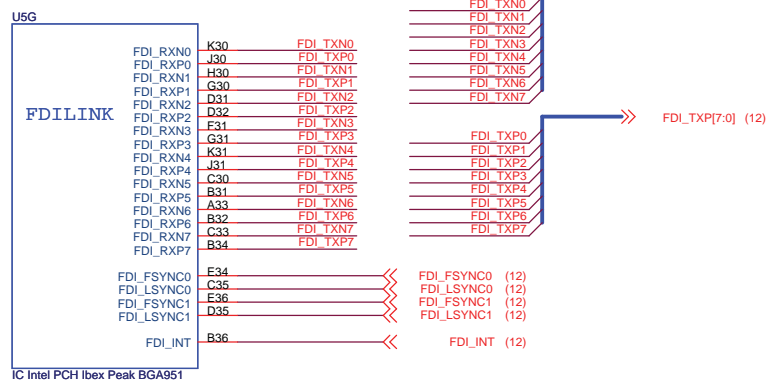
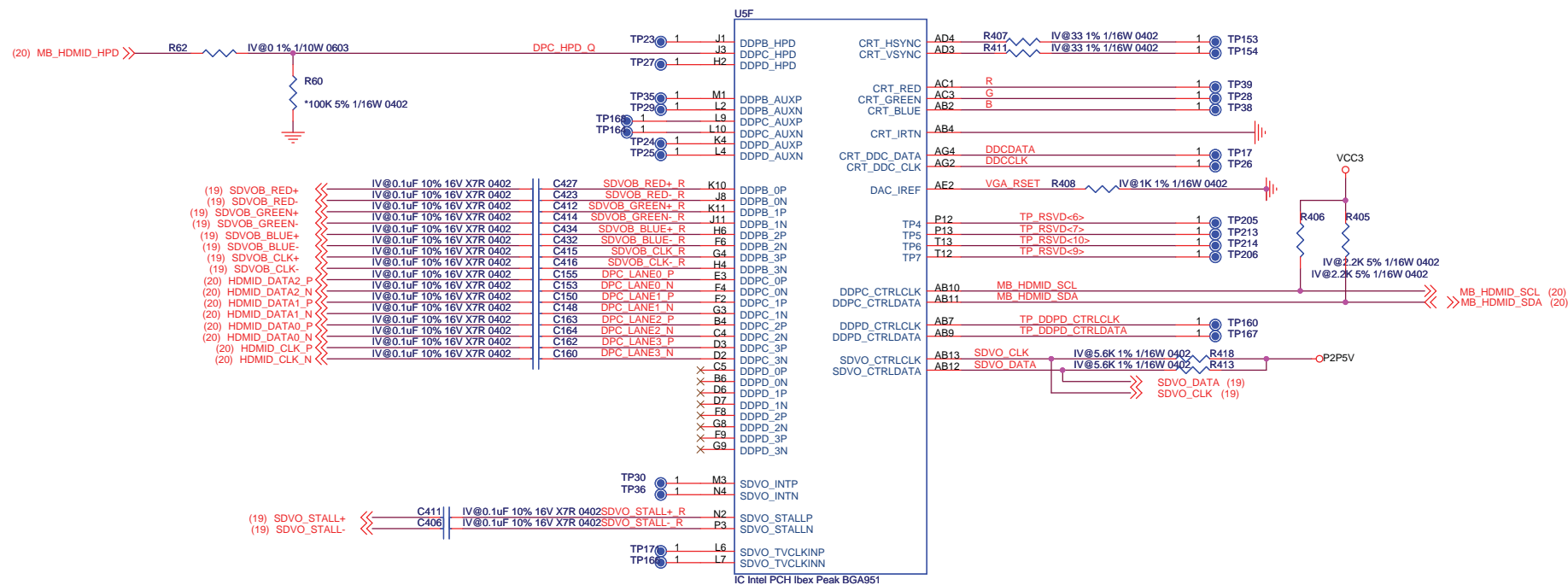


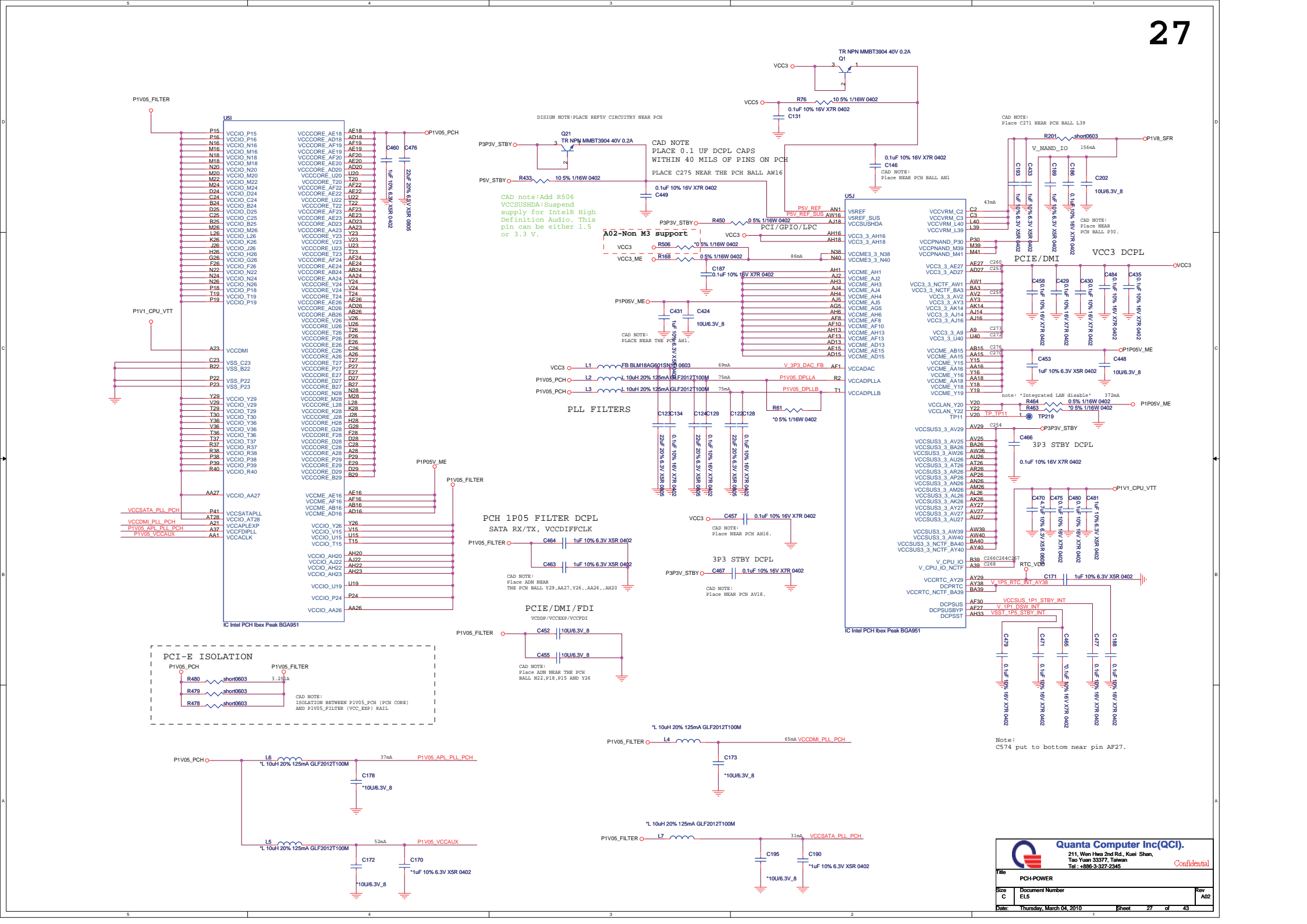
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Title: PCH-PCI		
Size: Custom	Document Number: EL5	Rev: A02
Date: Thursday, March 04, 2010	Sheet: 22 of 43	

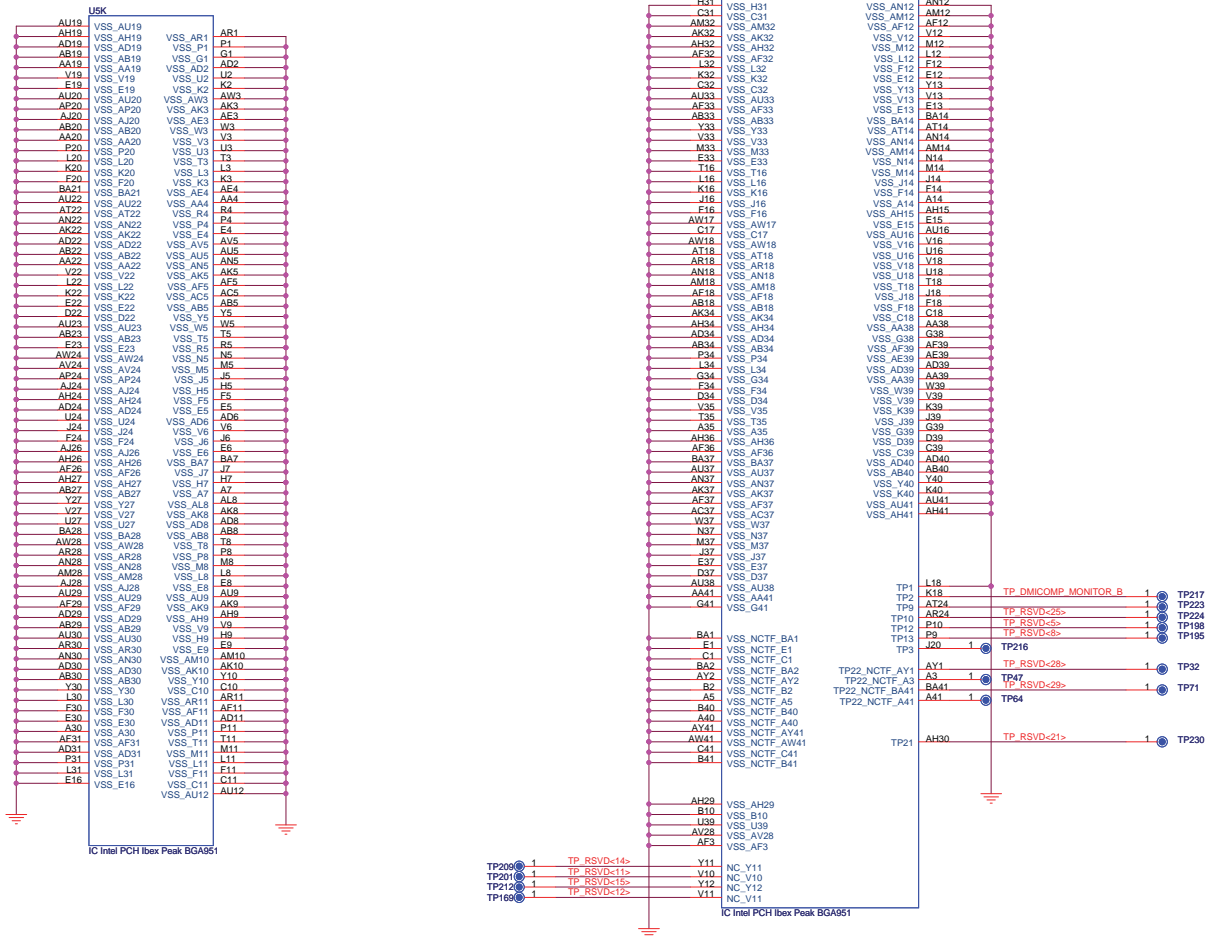




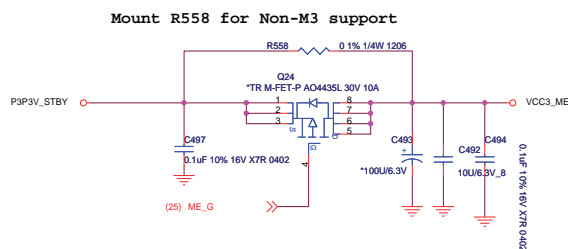
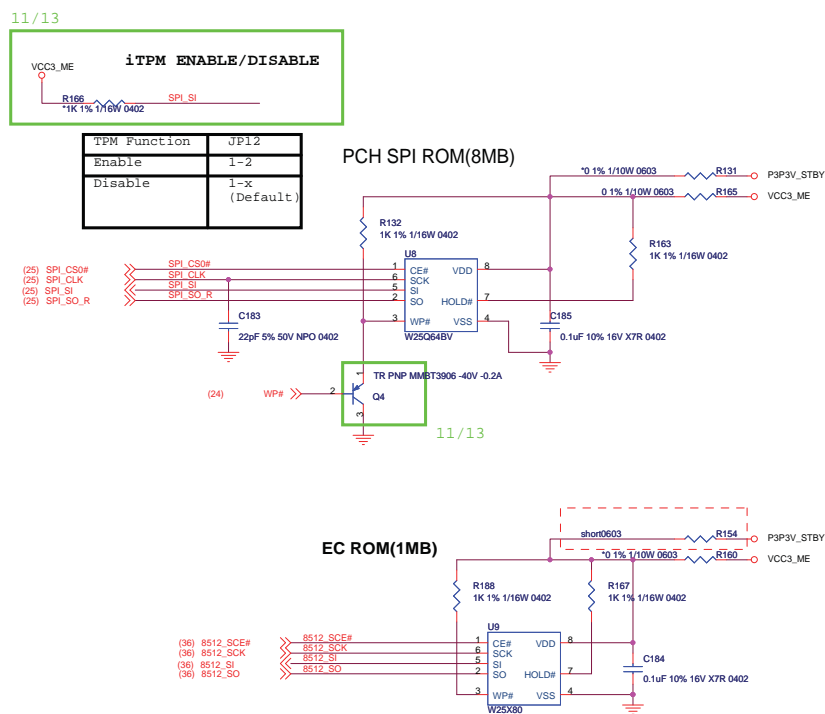
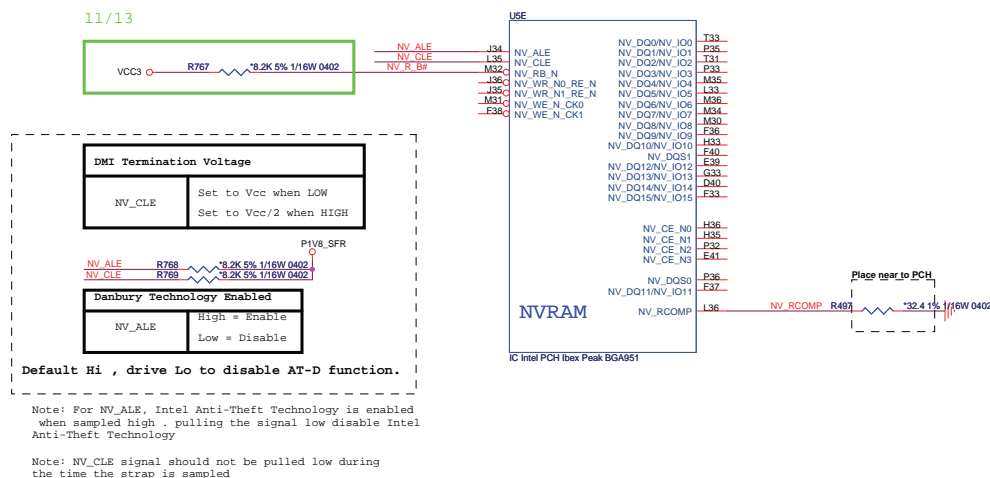






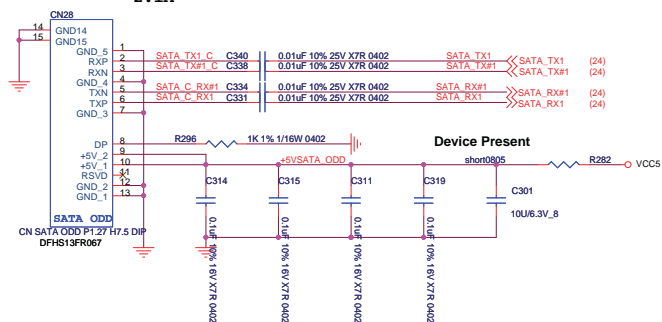


PCH - GND

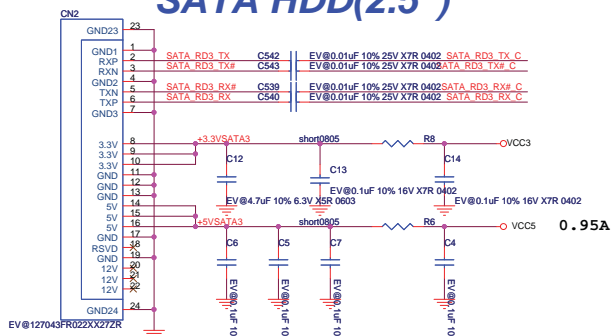


SATA ODD

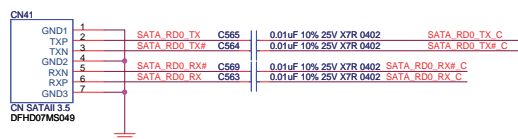
2.1A



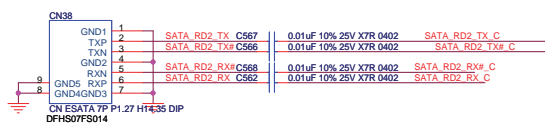
SATA HDD(2.5")



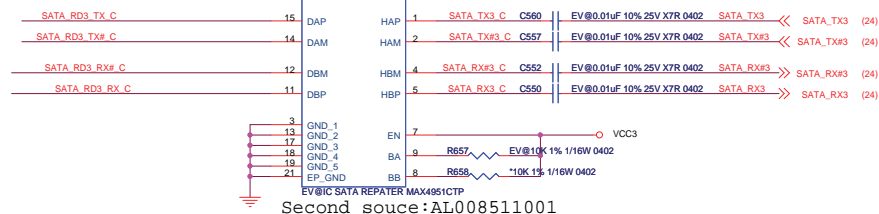
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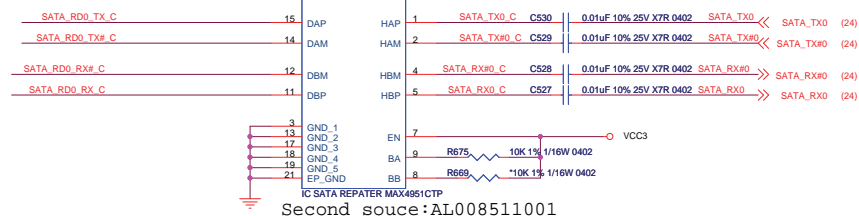
ESATA CONN



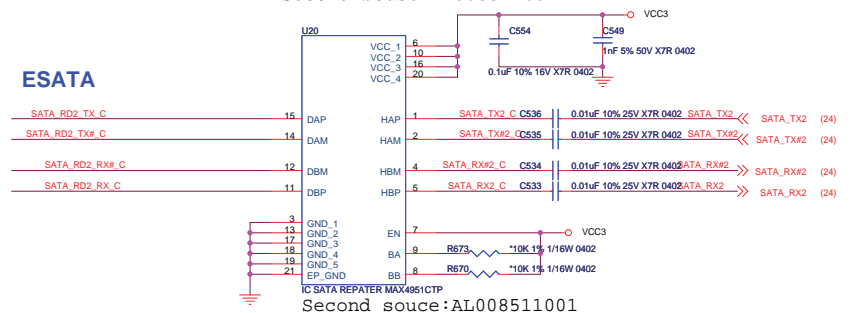
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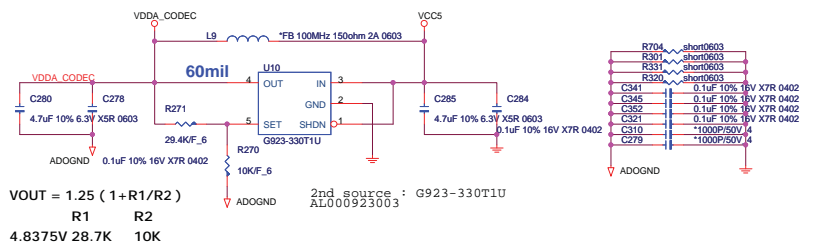
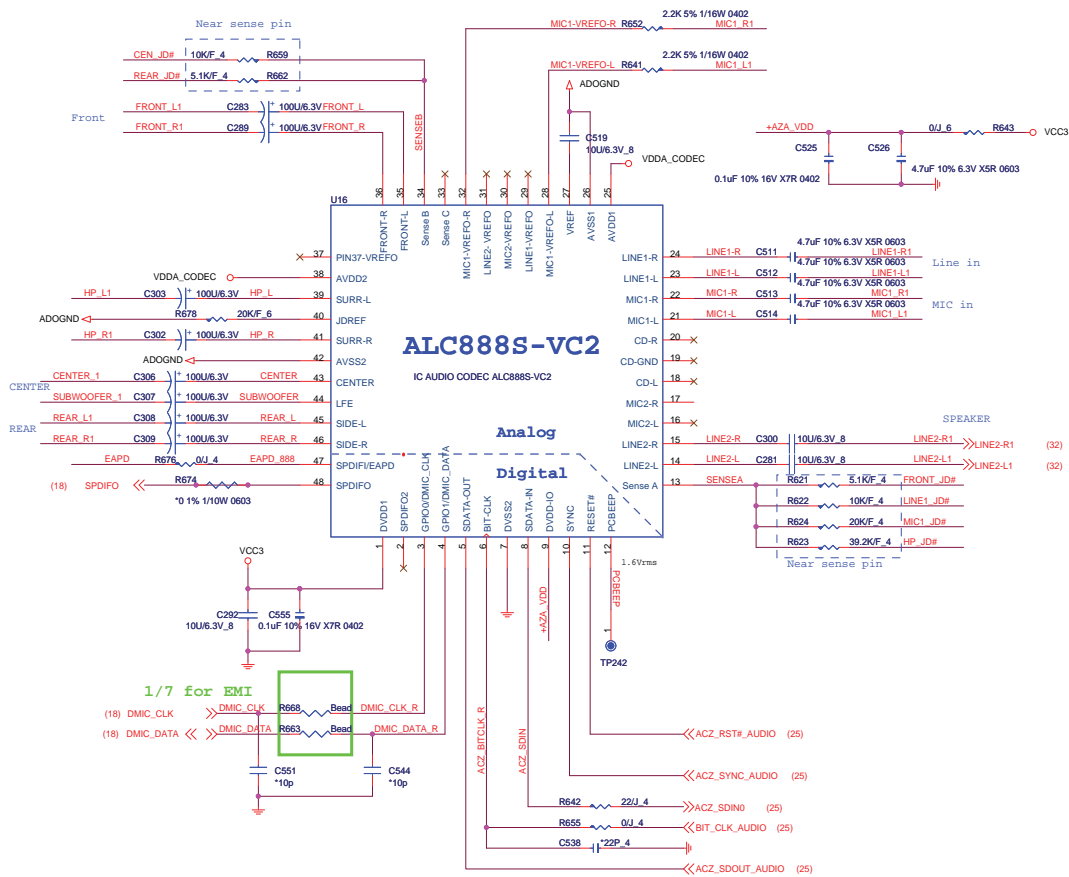
SATA HDD(3.5")



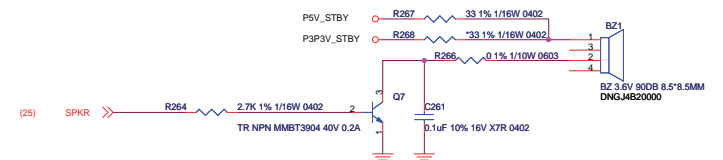
ESATA



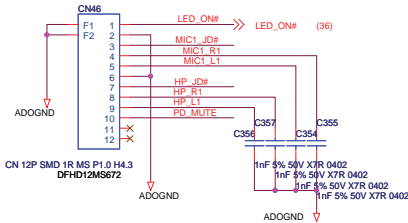
CODEC



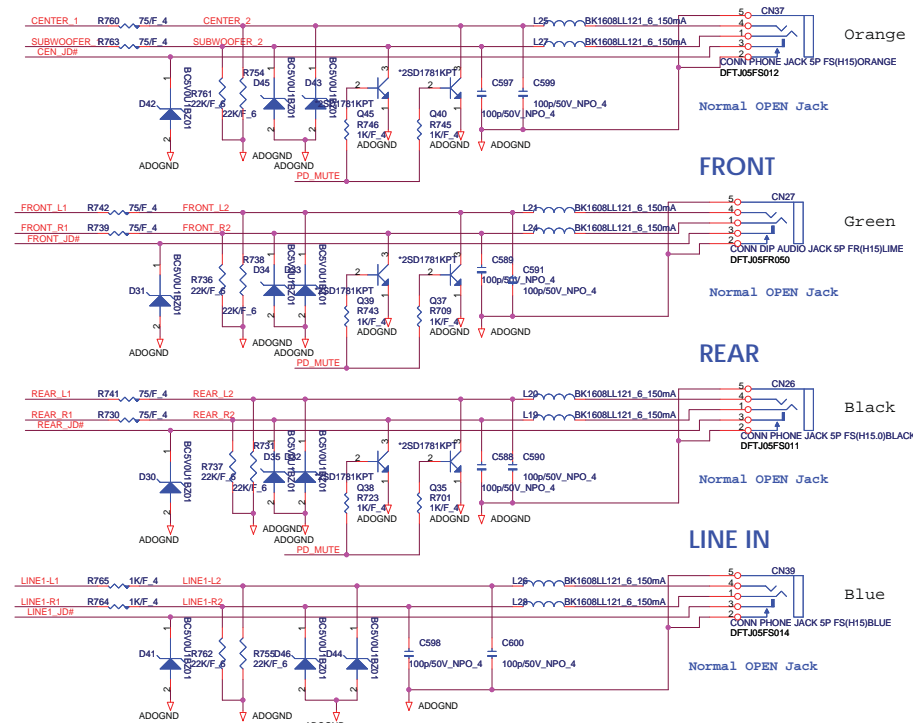
BUZZER



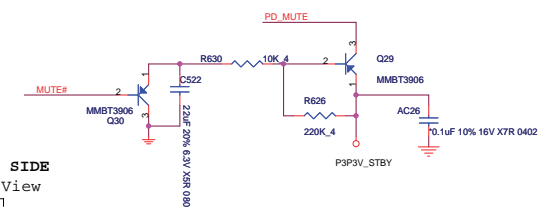
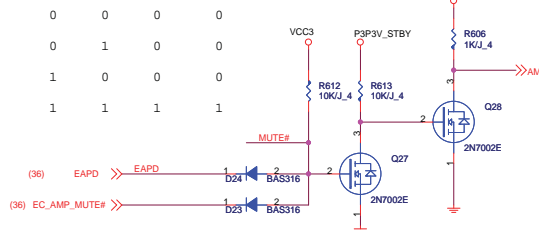
EXT. MIC & HP



CENTER & SUBWOOFER



MUTE



EC_AMP	MUTE#
0	0
0	0
1	1
1	1

	EAPD
0	0
1	1
0	0
1	1

#	AMP_ MUTE#
	0
	0
	0
	1

VCC3

MUTE

P3P3V

R612
10K/J_4

R6
10

STBY

>>AMP_MUTE#

13

(25) SPKR


R264 2.7K 1% 1/16W 0402

TR NPN MMBT3904 40V 0.2A

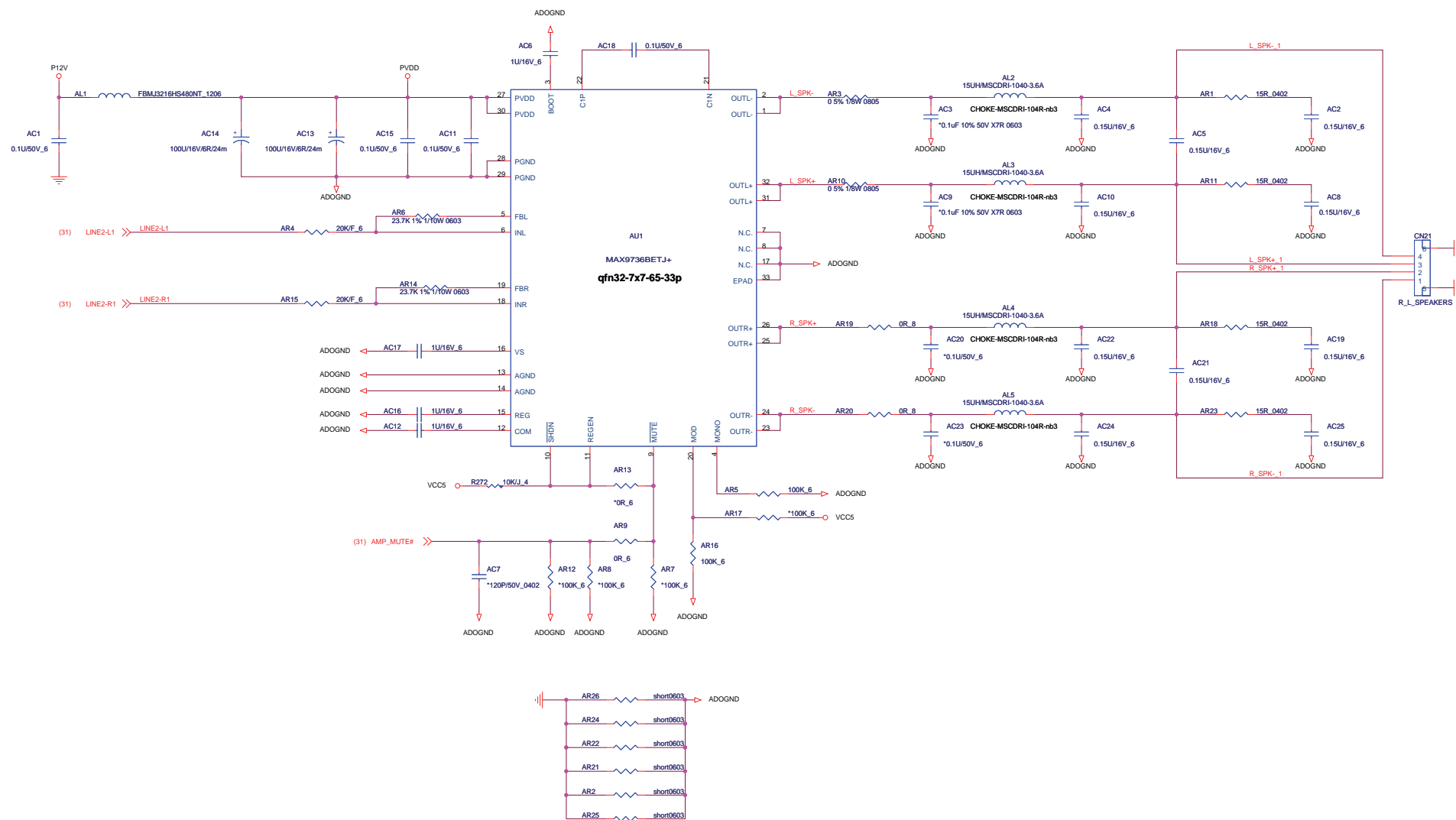
C261 0.1uF 10% 16V X7R 0402

BZ 3.6V 90DB 8.5*8.5MM DNGJAB20000

Figure 10 is a schematic diagram of the AD converter input circuit. It shows a 12-bit digital input (pins 10, 11, 12) connected to a 12P SMD 1R MS P1.0 H4.3 DFHD12MS672 resistor network. The circuit includes a PD_MUTE signal, a C356 capacitor, and a C357 capacitor. The input is connected to ADOGND. The output is connected to ADOGND through a 50V XTR 0402 resistor network.

 Quanta Computer Inc(QCI). 211, Wen Hwa 2nd Rd., Kwei Shan, Tao Yuan 33377, Taiwan Tel.: +886-3-327-2345		
Title AUDIO CODEC-ALC883/MIC/JACK		
Size	Document Number	Rev
C	ELS	A02

Speaker AMP.

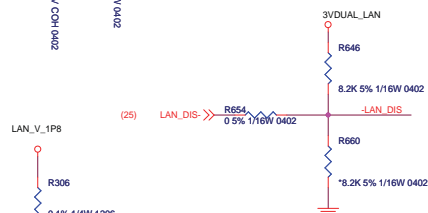




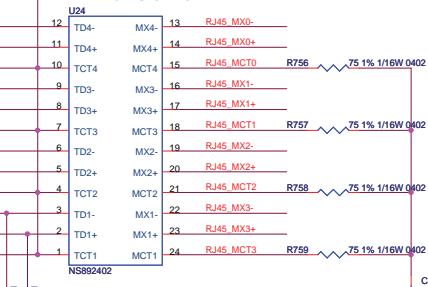
CRYSTAL SMD 25MHZ(+30PPM,20PF)E5FA25.00

HHE:BG625000486

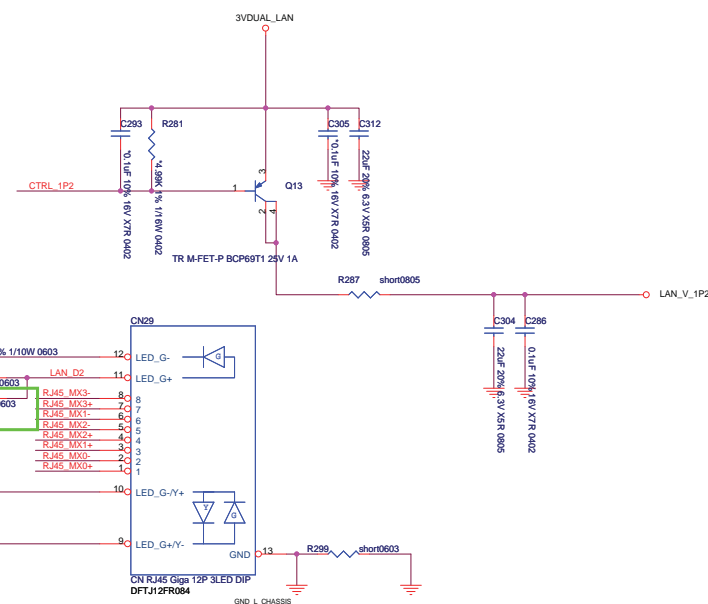
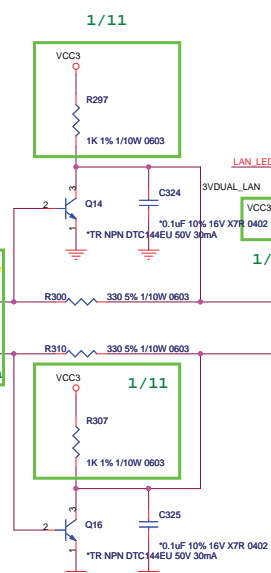
FEE:BG625000F21

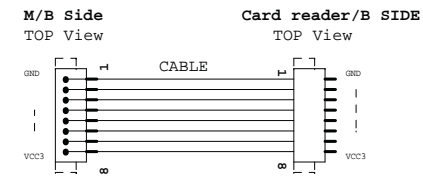
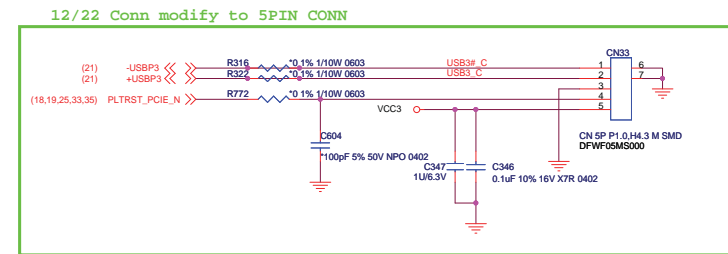
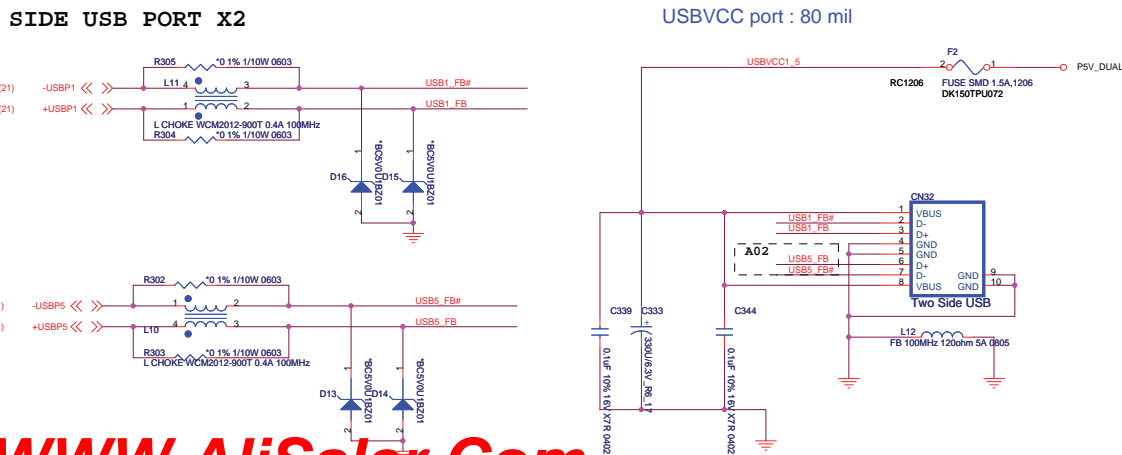
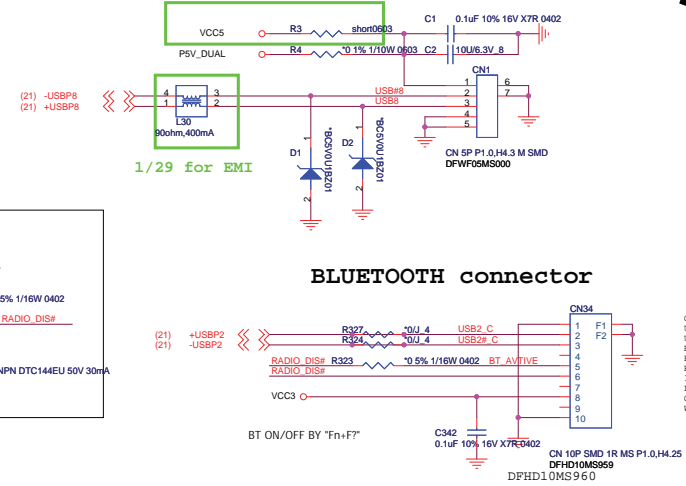


LAN Transformer

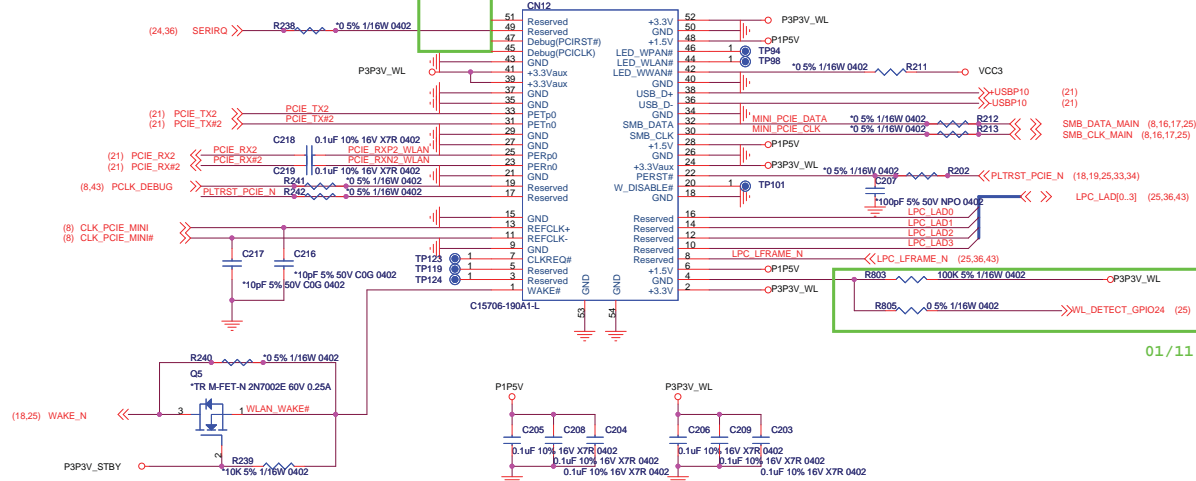


copy from EL7
trf-10-1-24p-nb3-->trf-10-1-24p-smt
for layout's request

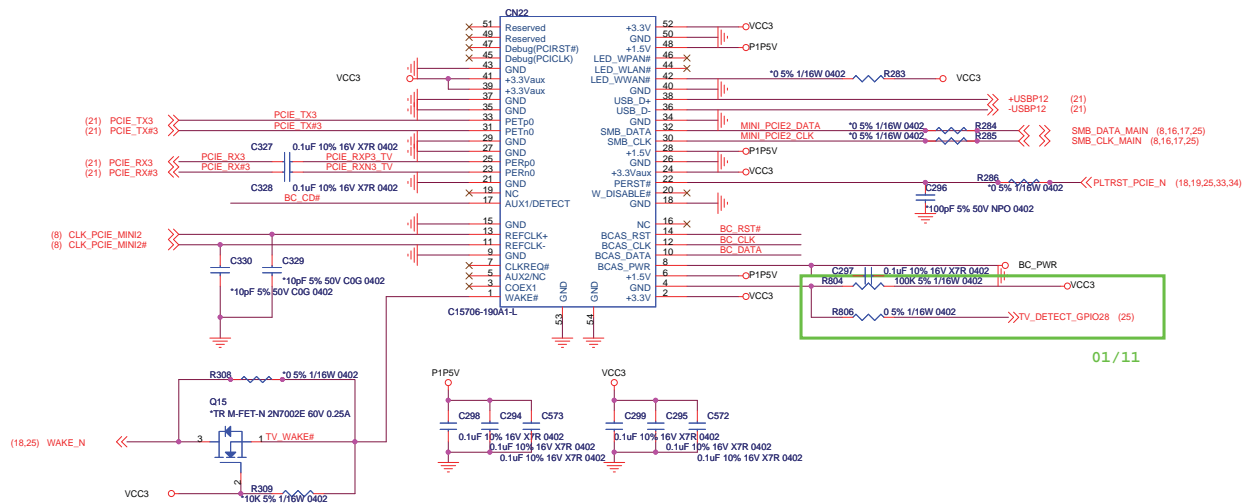




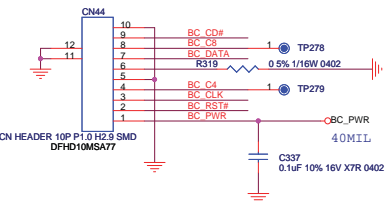
12/22 Wireless / 80 Port



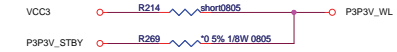
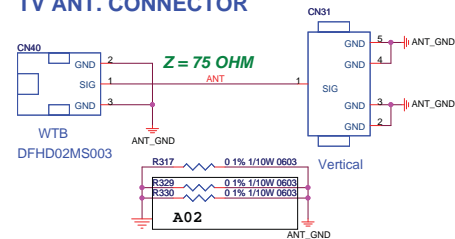
TV Card

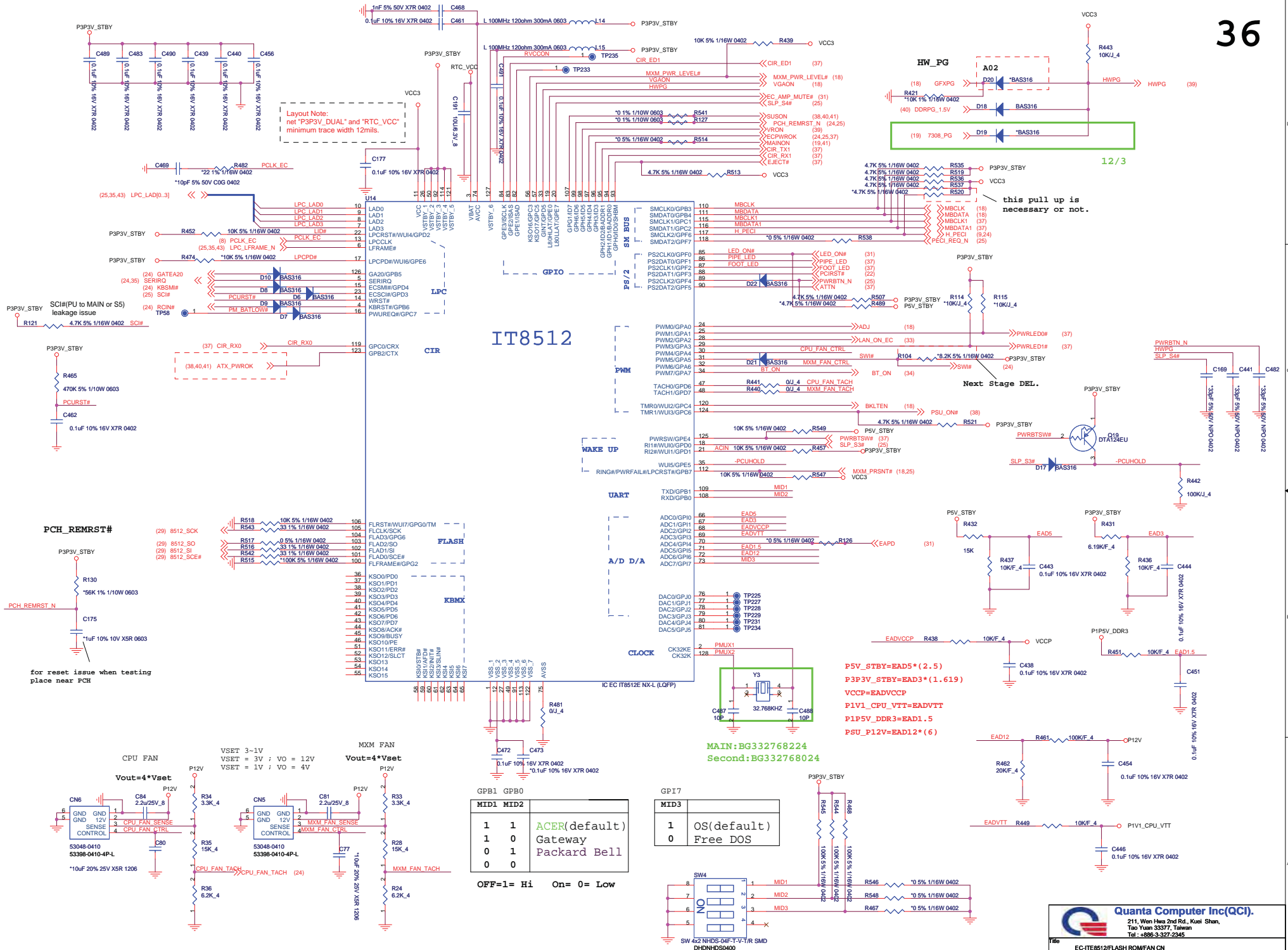


B-CAS CONN

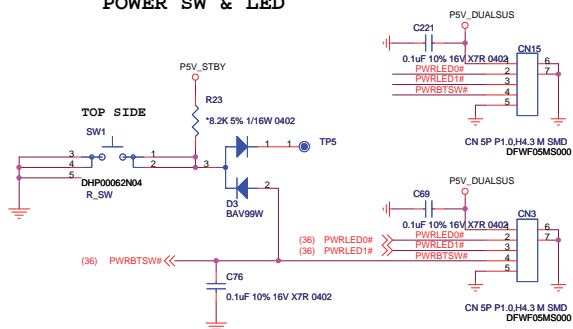


TV ANT. CONNECTOR

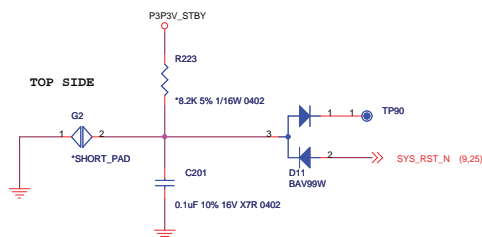




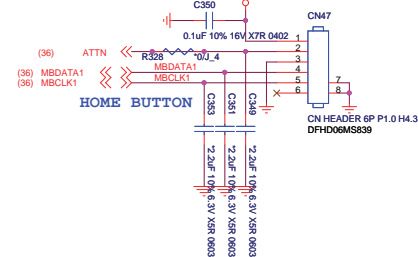
POWER SW & LED



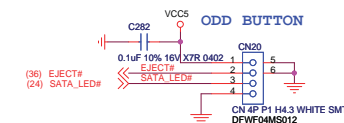
SYSTEM RESET



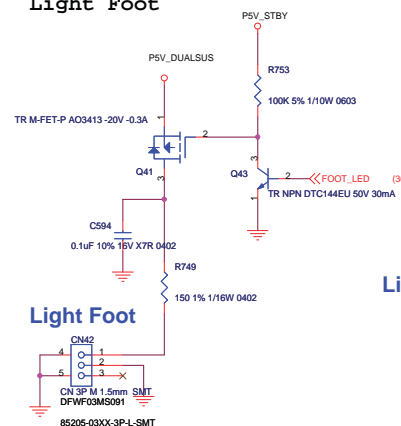
HOME **BUTTON**



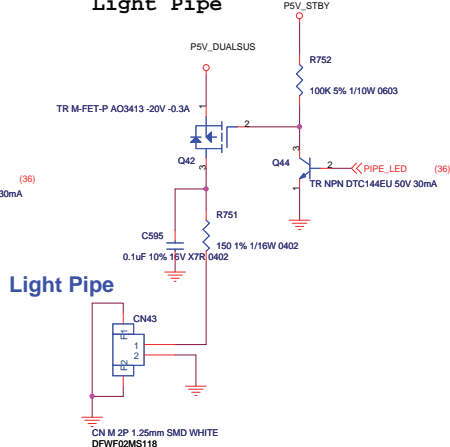
ODD EJECT



Light Foot



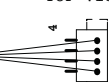
Light Pipe



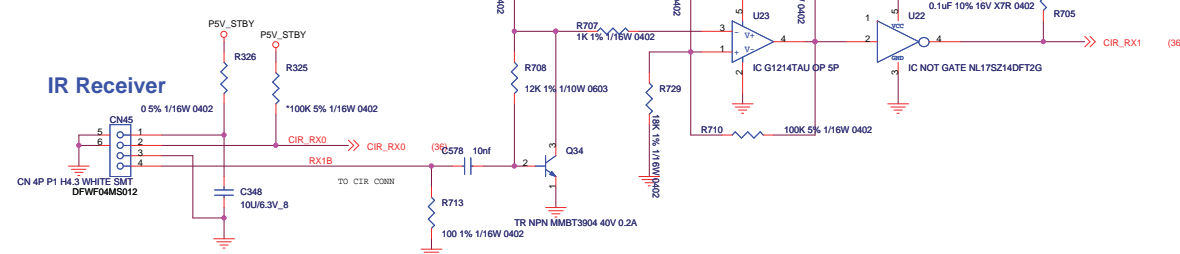
M/B Side
TOP View



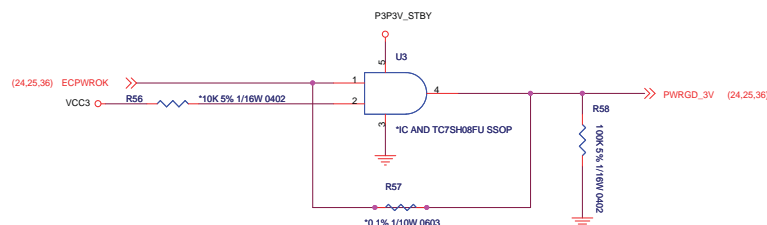
IR/B SIDE
TOP View



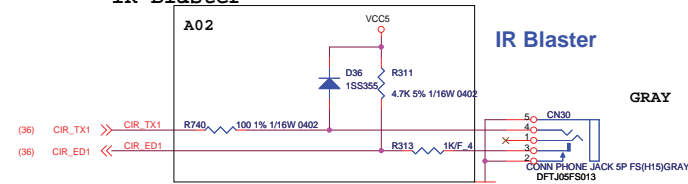
IR Receiver



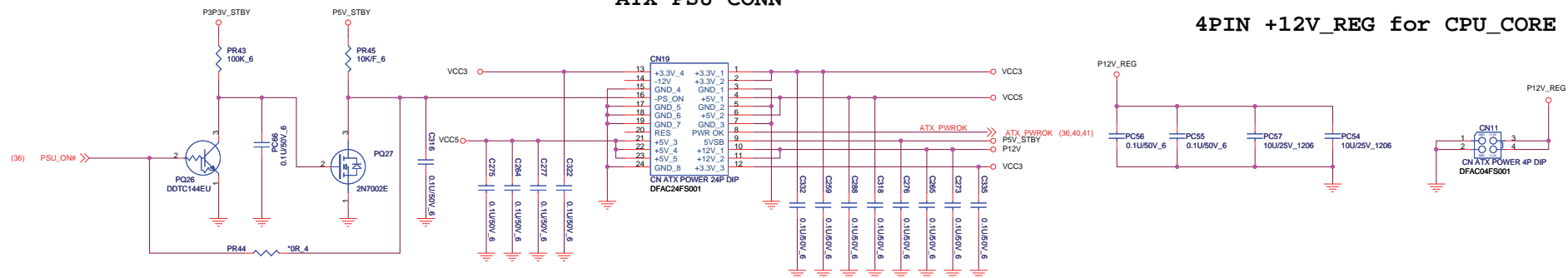
PCH POWEROK



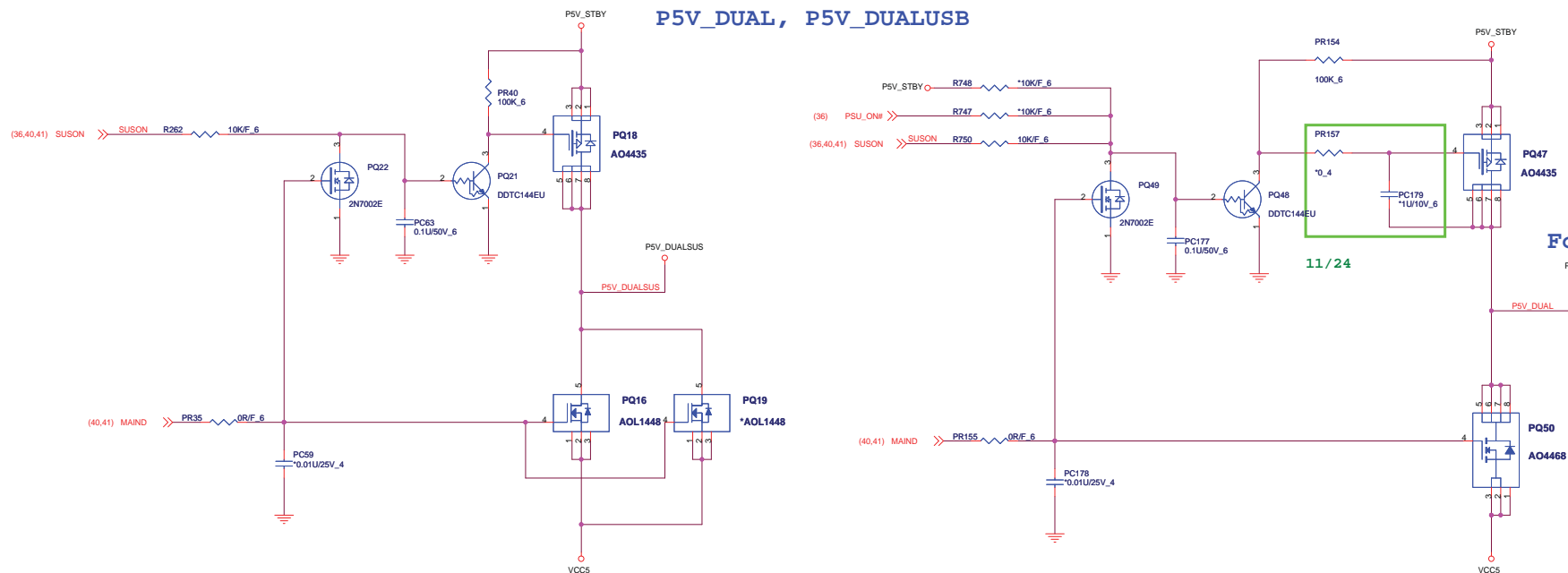
IR Blaster



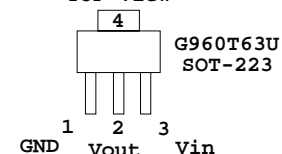
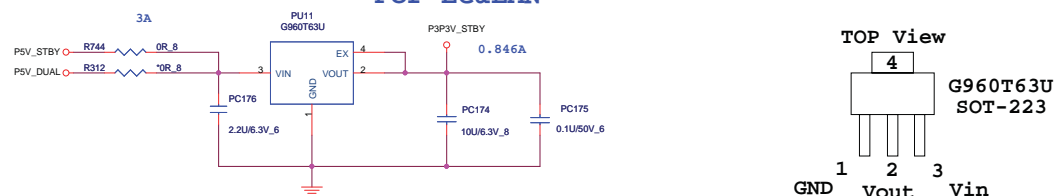
4PIN +12V REG for CPU CORE

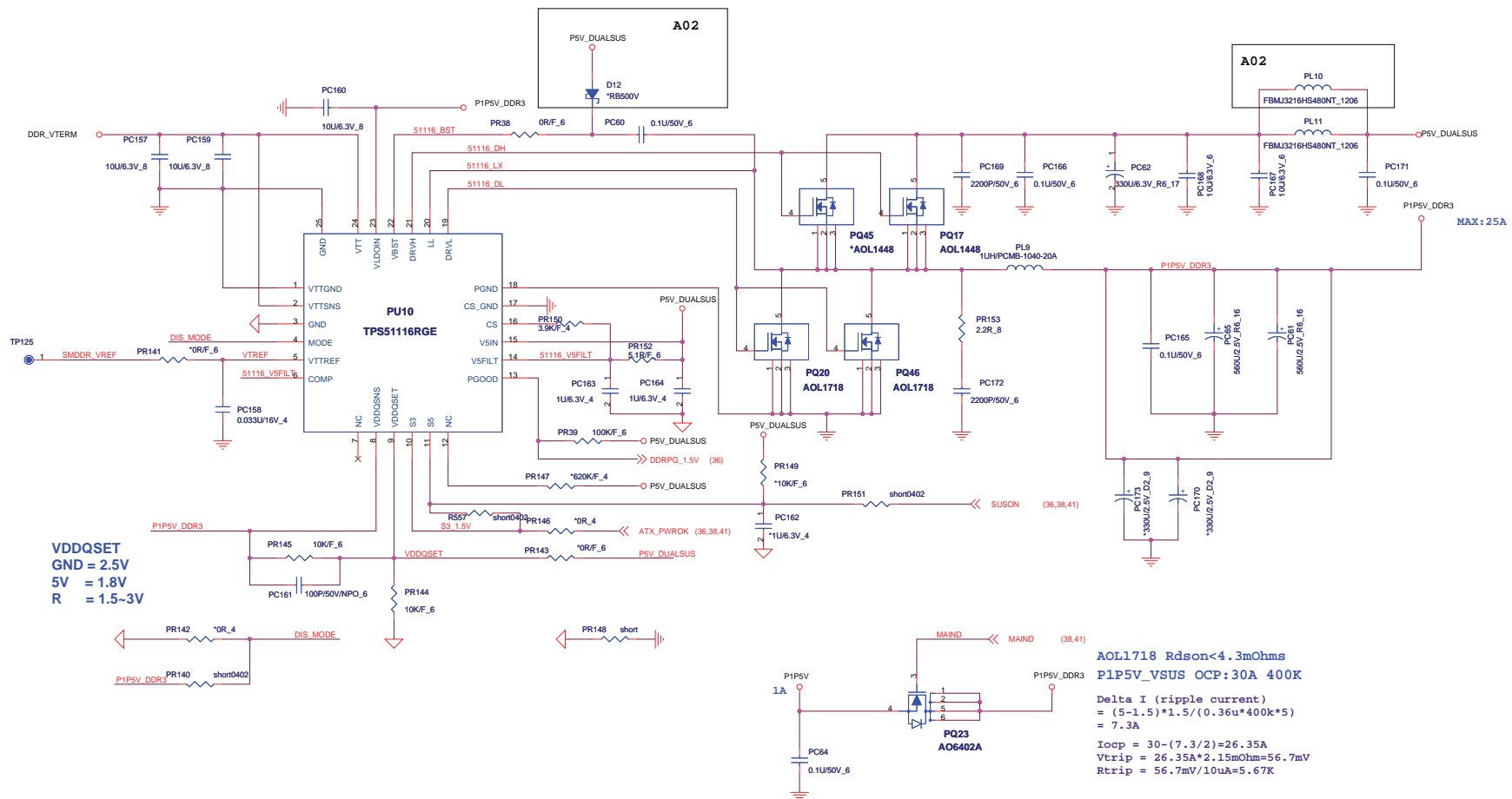


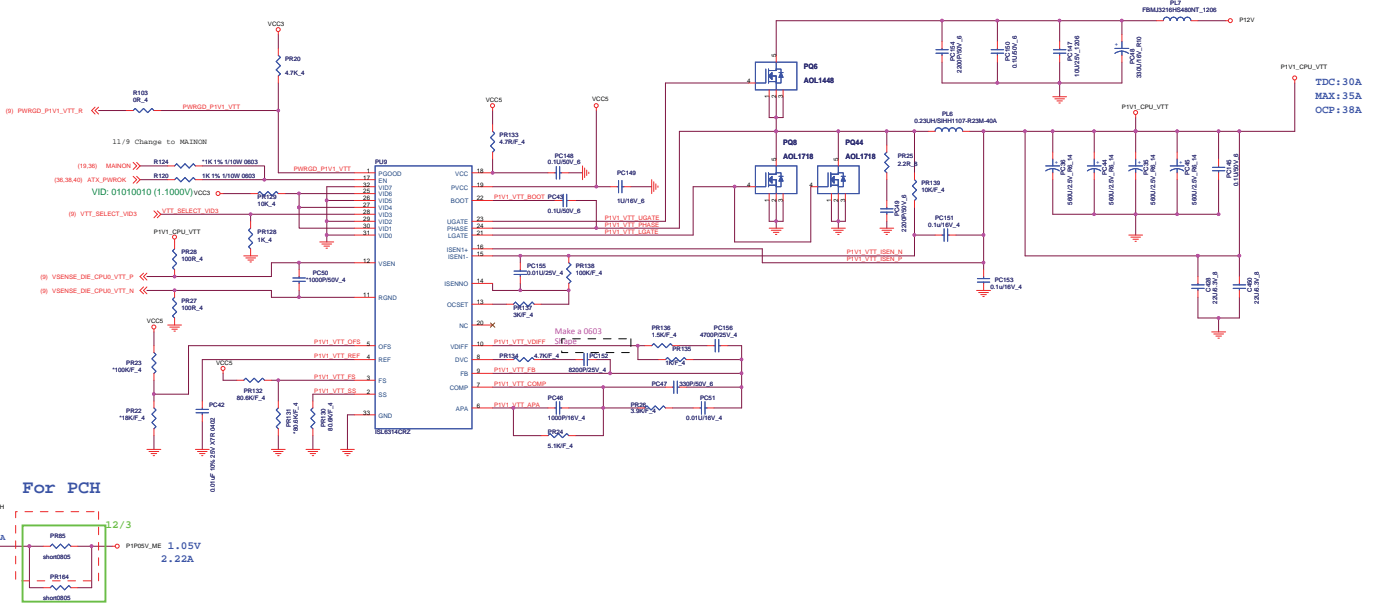
For USB



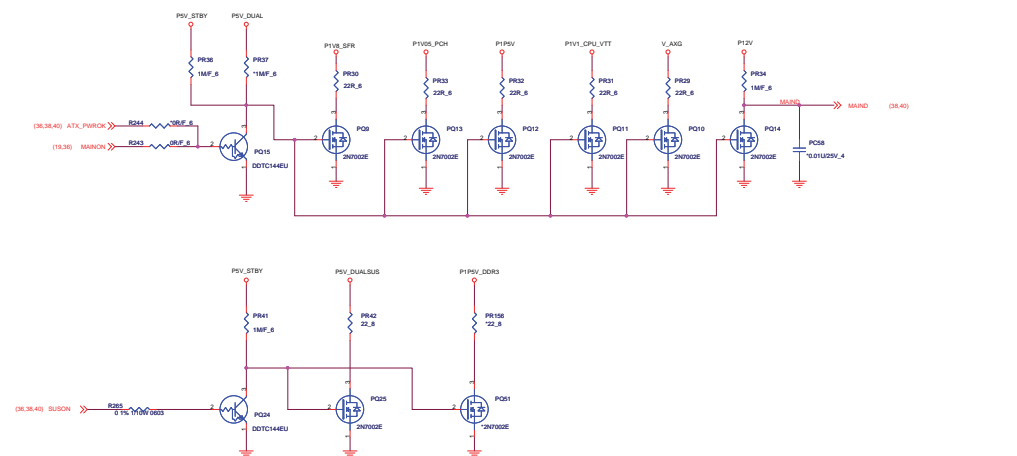
TOP View

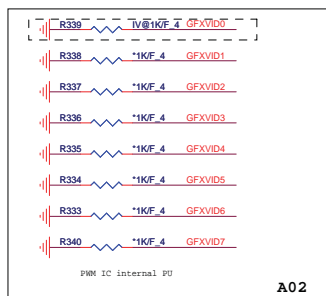




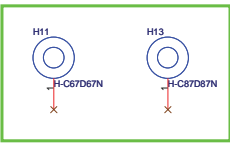


Short for Non-M3 support

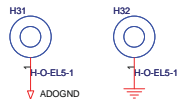
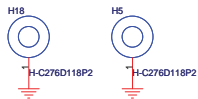
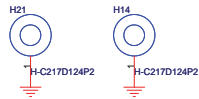
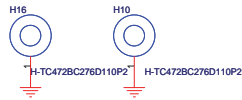
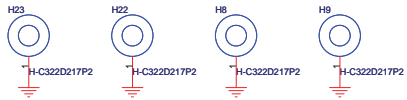
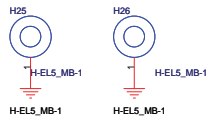
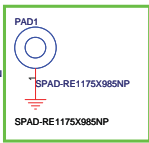




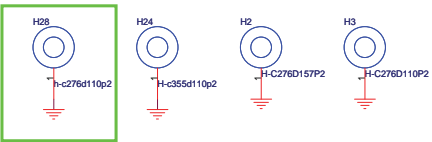
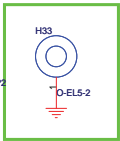
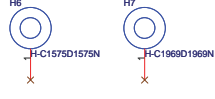
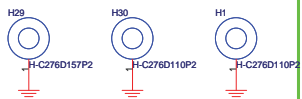
02/22 Change size for ME



01/08 Add PAD FOR EMI



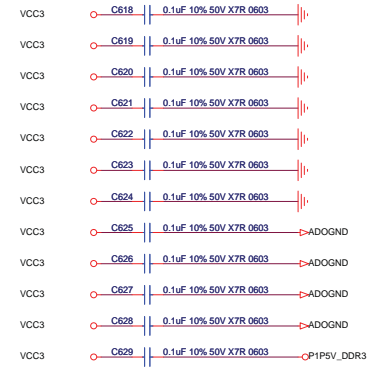
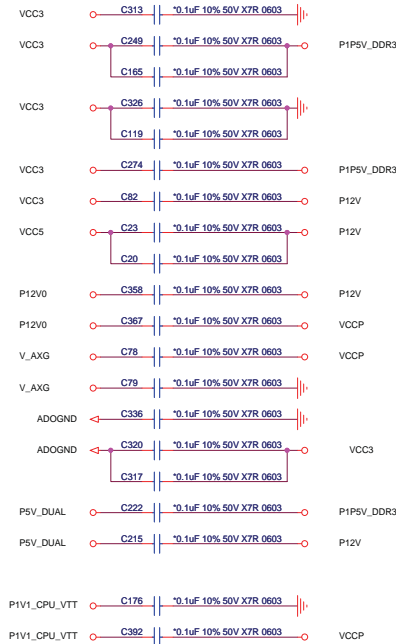
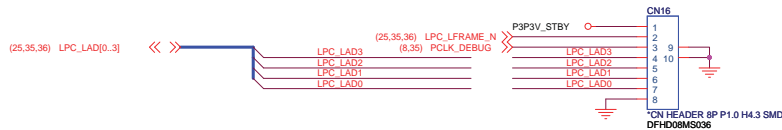
12/22



WLAN / TV

12/4

CONN(LPC Debug Card)



2/23 For EMI